The breaking point of modern processor and platform technology

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The quest for performance

Increased accuracy and detail of processing is expected
Constantly increasing demand for computing resources
Future upgrades of the LHC: data rates higher up to 2 orders of magnitude

Trends in HEP software

Significant (at least an order of magnitude) speedups possible through careful algorithmic and precision related considerations

In spite of being blessed with trivial parallelism, HEP code is very rarely making use of multi-threaded technologies to save memory
Post-initialization forking is a good start

Advanced, highly beneficial processor features remain unused, wasting capacity: 30% wasted for hardware threading, over 75% for vectors 64-bit not used widely

Complex HEP C++ code produces binaries which are not processor-friendly: processors are under-utilized, to the point where 75%-90% of theoretical execution capacity in a core is wasted

Platform and architecture of choice

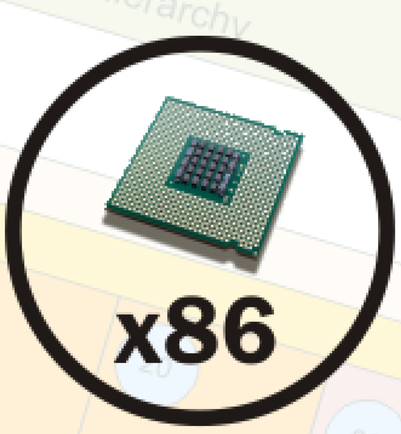
Excellent handling of high level languages

Incrementally growing number of cores

Well established family of compilers

Growing amount of functional units

Growing importance of hardware threading



Vector space is likely to grow in length

Little hopes for frequency scaling

Open possibility: Intel KNF

Open possibility: Intel SCC

Many-core platform scalability issues

Maximum 10 more years of life with traditional materials

Trends in x86 hardware

Multi-core processors are standard, however whereas core increase was geometric, it will be incremental

Example history: 2, 4, 8, 10
for Intel Core 2, Penryn, Nehalem and Westmere

Due to various inter-core issues and platform bottlenecks, many-core systems don't allow for software scaling like the multi-core ones

An expansion in functional unit amount and capacity is likely: e.g. vector space is likely to grow in length
Hardware threading is a popular and supported feature

Moore's Law is facing some significant challenges
Scaling limit foreseen in 2020 with feature sizes of 10 Angstrom
TDP constraints forbid frequency scaling

Experimental technologies

Intel Knights Ferry:
32 in-order x86 cores
128 threads (4-way hardware threading)
512-bit vectors

Intel Single-chip Cloud Computer:
A tiled cluster of 48 IA cores with no shared memory
Packet-based message passing to neighbors only
Advanced frequency and voltage regulation