Dynamically Adaptive Header Generator and Front-End Source Emulator for a 100 Gbps FPGA based DAQ

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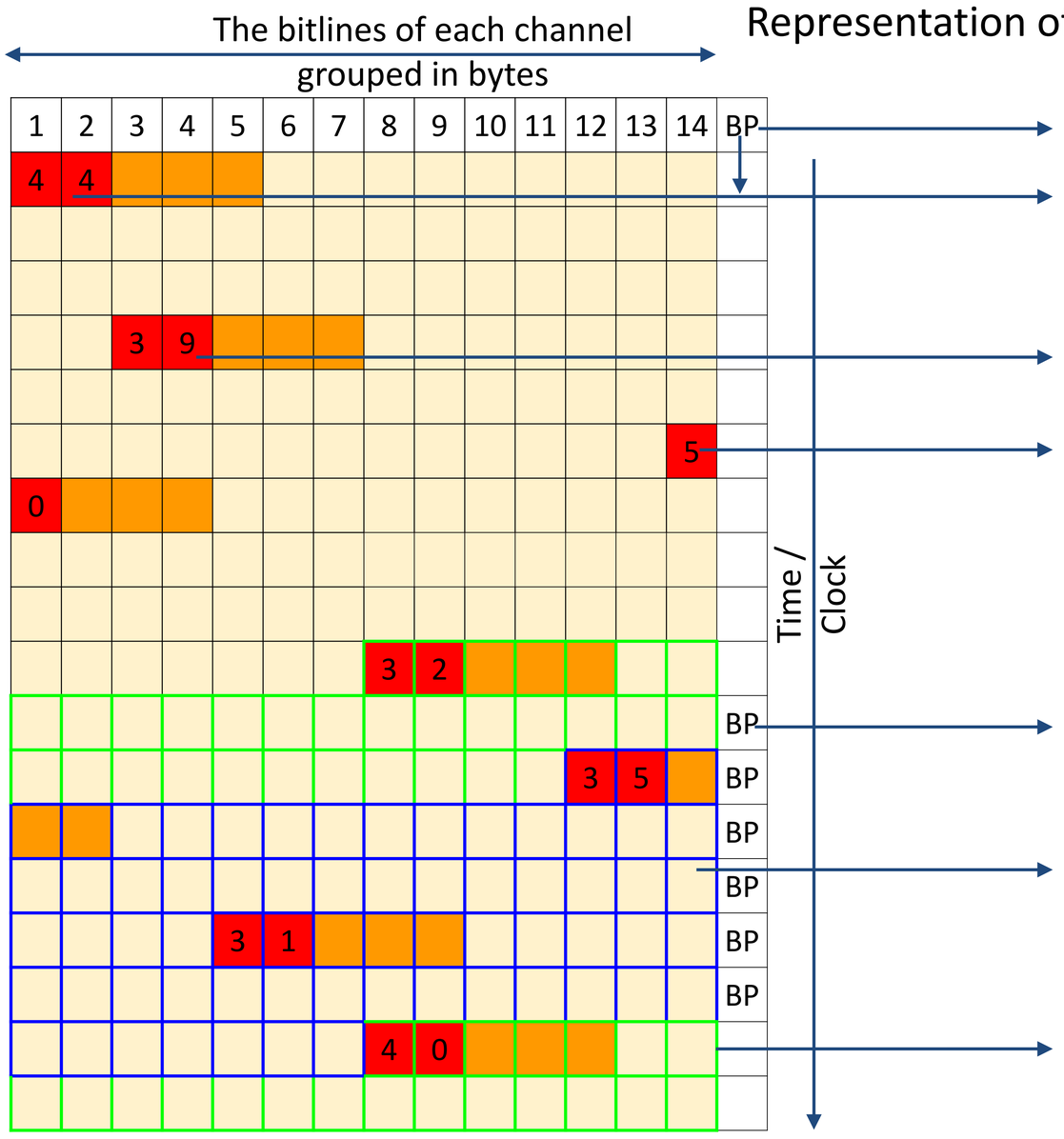
The Grand Challenge for proposed upgrade of LHCb experiment:

- 500 Data sources each generating data at 100 Gbps.
- Requires an FPGA DAQ module that
  - handles data generated by the experiment
  - dynamically adapt to potential inadequacies of other components
  - maintain real time operation while at the same time maintaining system stability and overall data integrity

The Header Generator module is used to packetize the streaming data from the detector's Front-End electronics before it is sent to the PCs for further processing. The objective is to create a meta header or an index by creating packets out of 100s of small event dataset. This Header contains the total length of the packet, i.e. the sum of lengths of the individual datasets, the length of the largest dataset and a few other details calculated from information in the stream.

The Source Emulator generates the data stream that becomes the test input for Header Generator.

Breakdown of major challenges for this module



Representation of the data stream

Presence of Back Pressure from downstream modules

Header with length of dataset - critical to this module

Non Deterministic dataset length

Critical Header info split across lines/clock cycles

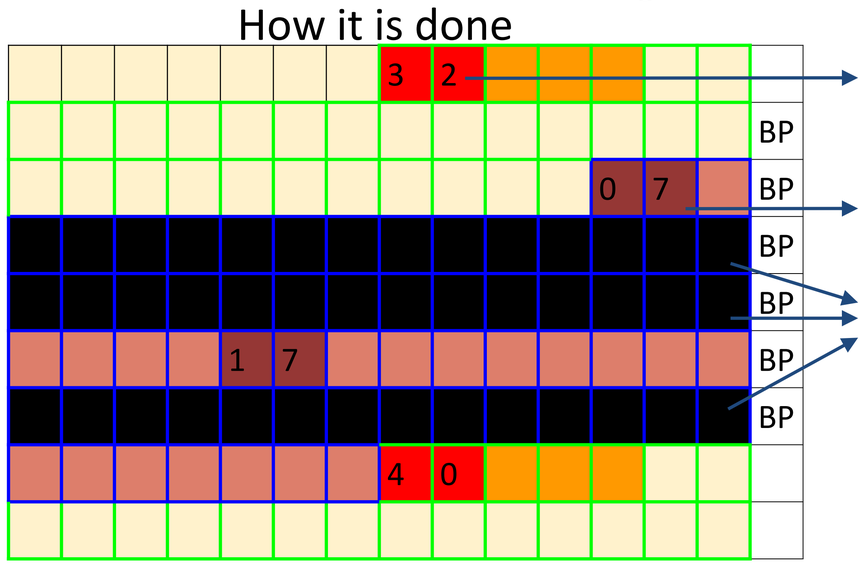
Part of dataset has already passed thru the module when back pressure detected - Complete the processing of current dataset

Drop data in controlled fashion, Generate new stream on the fly, Continue Header generation, Maintaining overall data integrity, All in Real-Time!

And when back pressure eases, continue as if nothing happened

Balancing Hard Real-time with Data Integrity and System Stability

How it is done

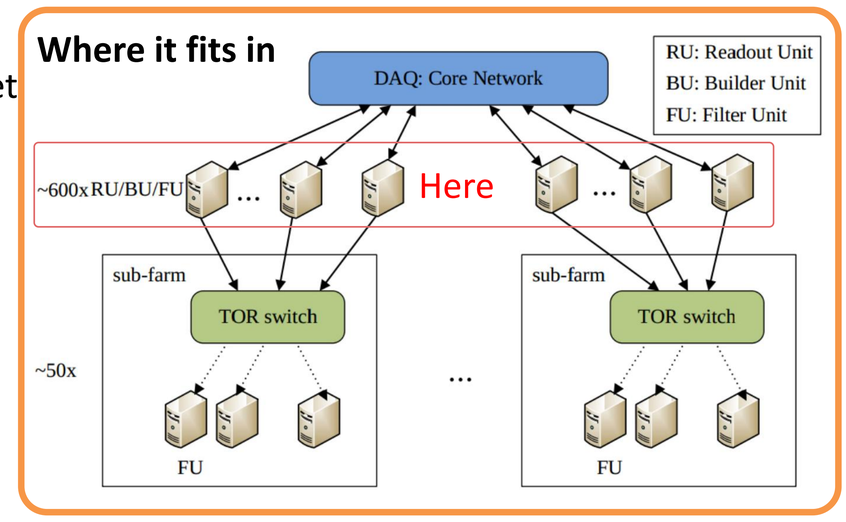


The current dataset length and its offset is used to calculate the offset of next header

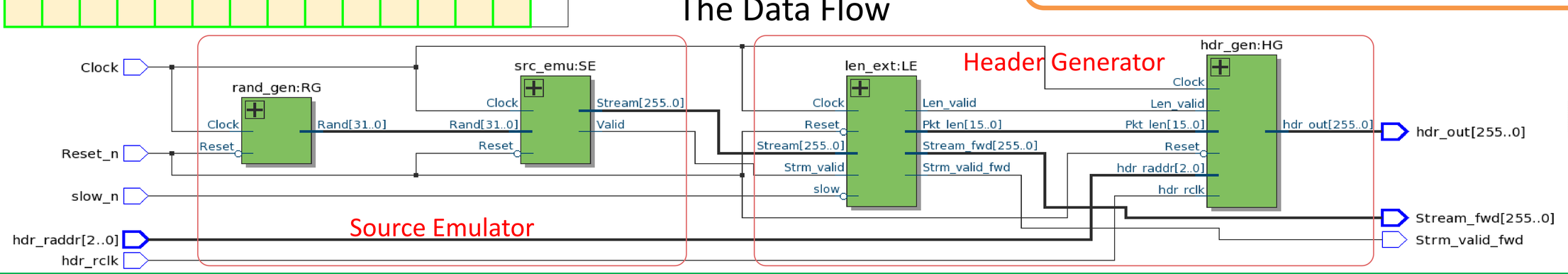
Dynamically rewritten header for shorter invalid packets

Lines that are discarded entirely

Where it fits in



The Data Flow



Results: This implementation capable of > 50Gbps. 100Gbps possible with wider & multiple pipelines, timing optimizations and newer devices.

Flow Summary

Flow Status	Successful - Tue May 06 14:14:28 2014	Logic utilization	< 1 %	Total block memory bits	4,096 / 18,579,456 (< 1 %)
Quartus II 64-Bit Version	13.1.0 Build 162 10/23/2013 SJ Full Version	Combinational ALUTs	984 / 282,880 (< 1 %)	DSP block 18-bit elements	0 / 1,040 (0 %)
Revision Name	header_generator_w_discard	Memory ALUTs	0 / 141,440 (0 %)		
Top-level Entity Name	test_top_w_discard	Dedicated logic registers	889 / 282,880 (< 1 %)		
Family	Stratix IV	Total registers	889		
Device	EP4SGX360KF40C2	Total pins	7 / 888 (< 1 %)		
Timing Models	Final	Total virtual pins	517		

Slow 900mV 85C Model Fmax Summary

	Fmax	Restricted Fmax	Clock Name
1	212.31 MHz	212.31 MHz	Clock
2	783.09 MHz	550.06 MHz	hdr_rclk

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