Simulation and Design of Si-Photonic Mach-Zehnder Modulators for radiation hardness testing

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PH-ESE-BE student seminar

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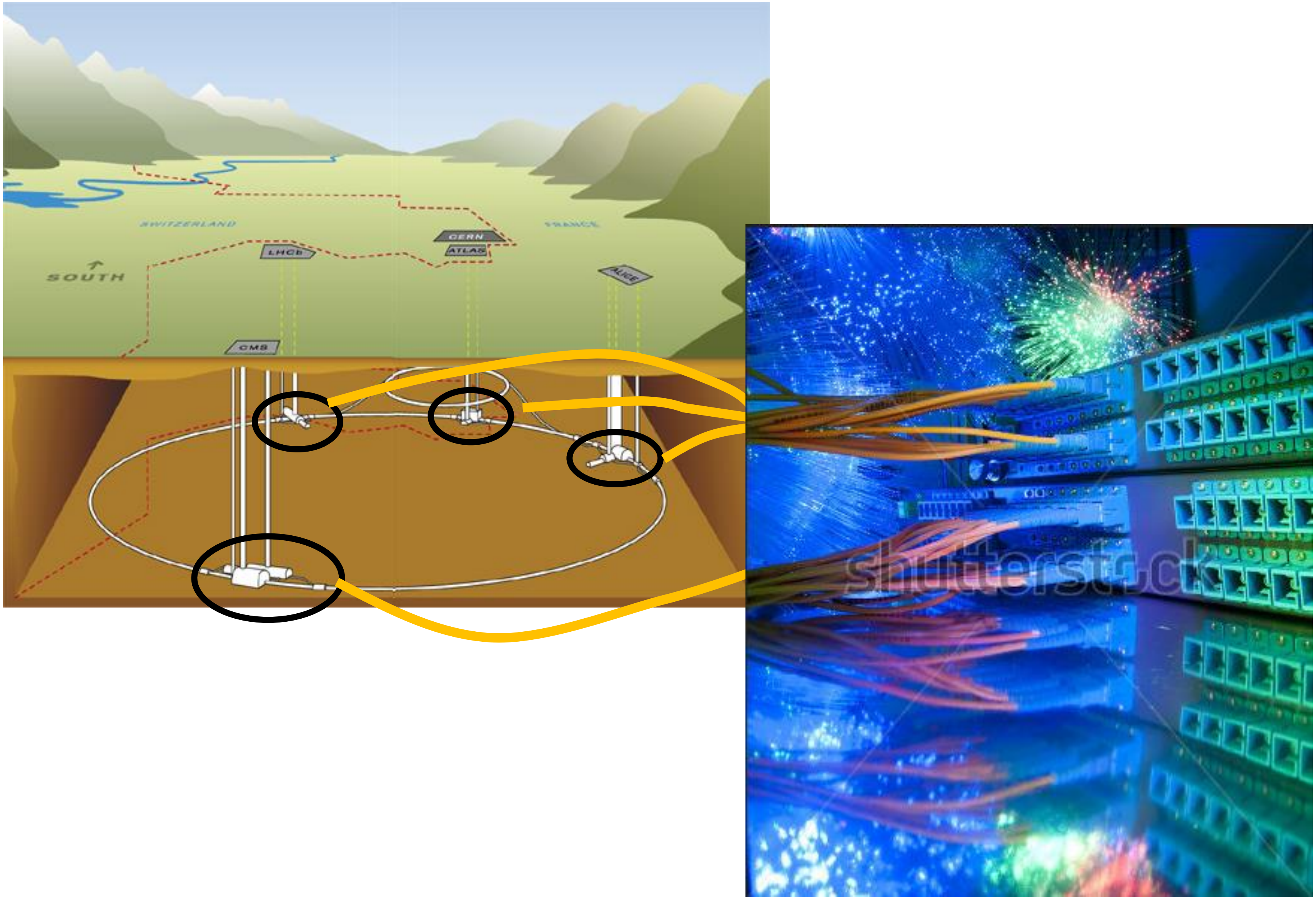
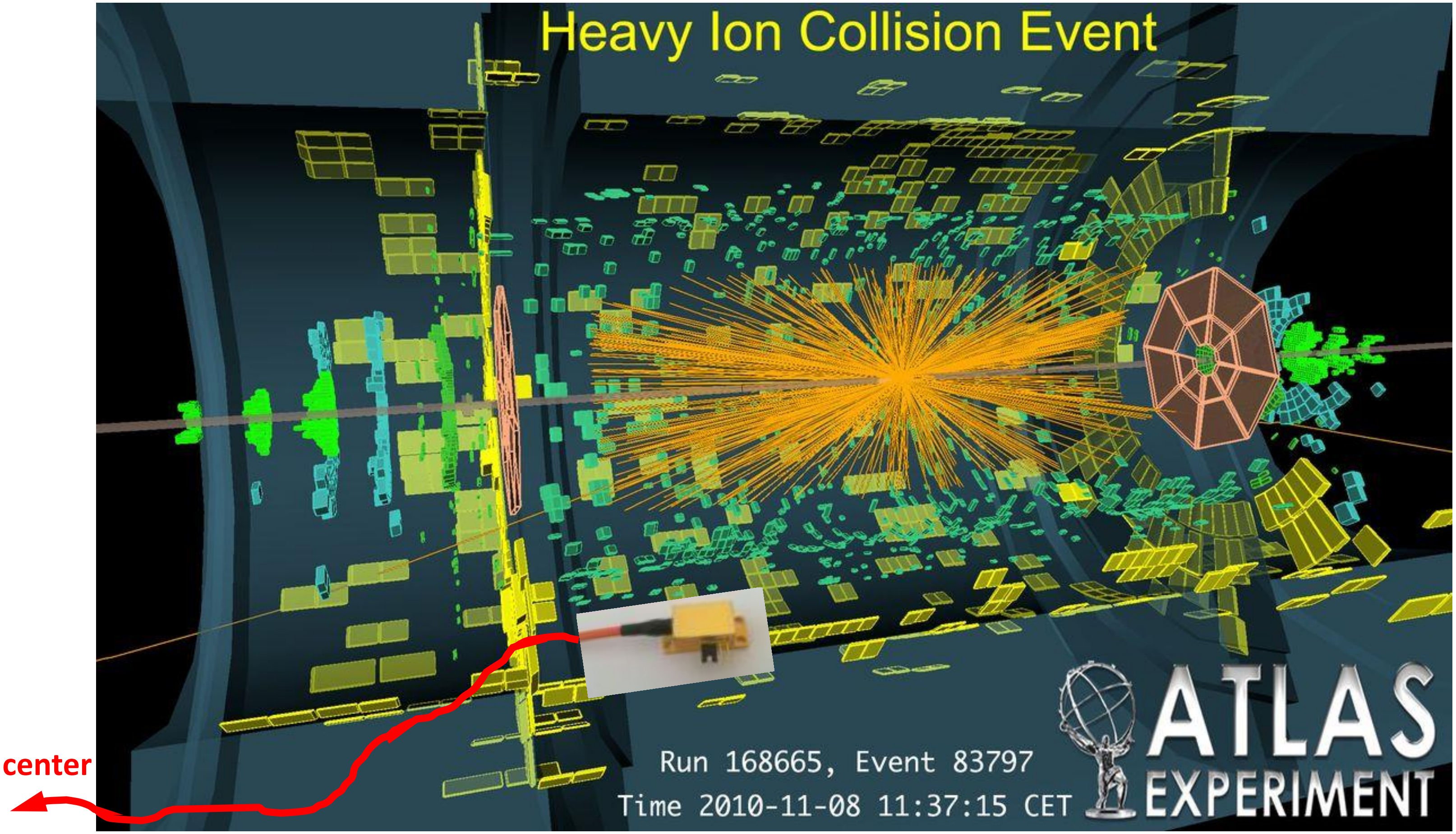
Outline

- Motivation
  - Why silicon photonics for CERN?
- Short theoretical introduction
  - Mach-Zehnder modulator device principles
  - Implementation in silicon
- How can we fabricate our own prototypes?
  - Multi-project wafer runs
  - Advantages and restrictions
- Device simulations – How to find the best design parameters?
  - Interplay optical and electrical simulations
  - Identification of design to be realized
- Mask design
  - What is included in the chip?
  - What to consider regarding specific foundry technology?

Fiber optic links are installed to transmit collision data from detector to data center



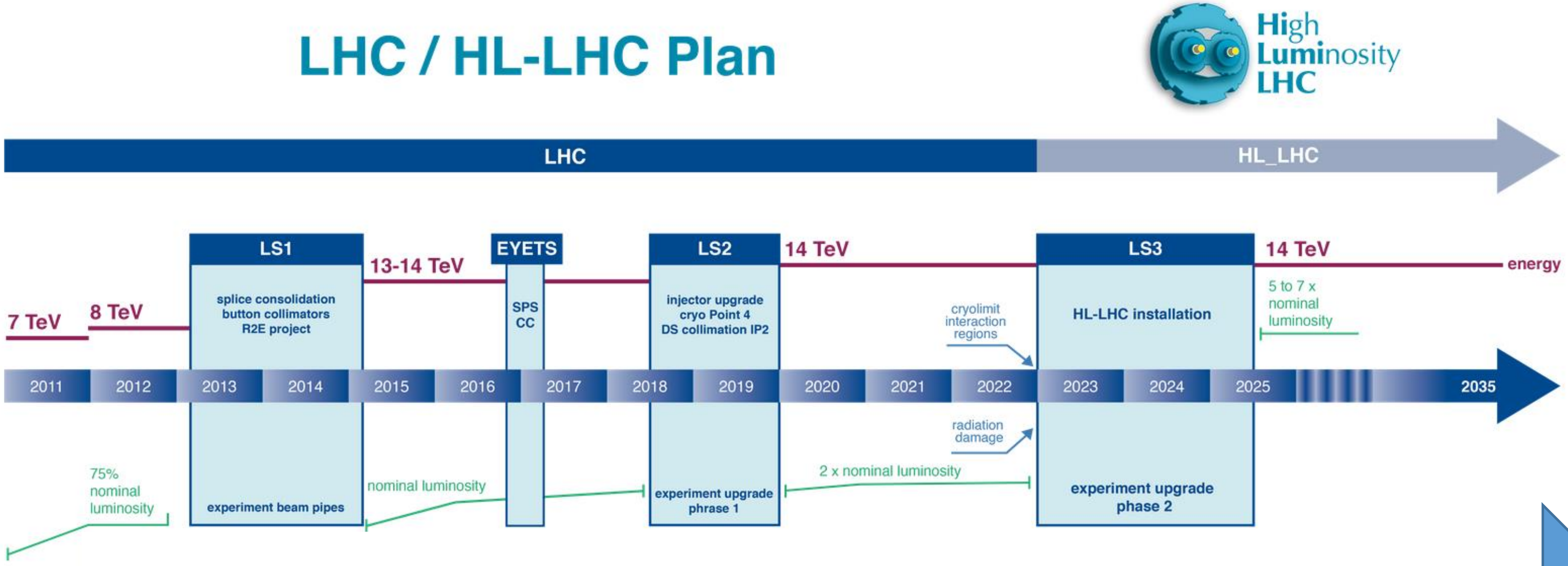
Radiation in detector requires special component design



to data center

Particles created in collision (e.g. neutrons, x-rays) impinge on components installed in Large Hadron Collider (LHC) detectors and might damage them.

LHC upgrades pose new challenges to component design



number of colliding particles

particle energy

more measurement data

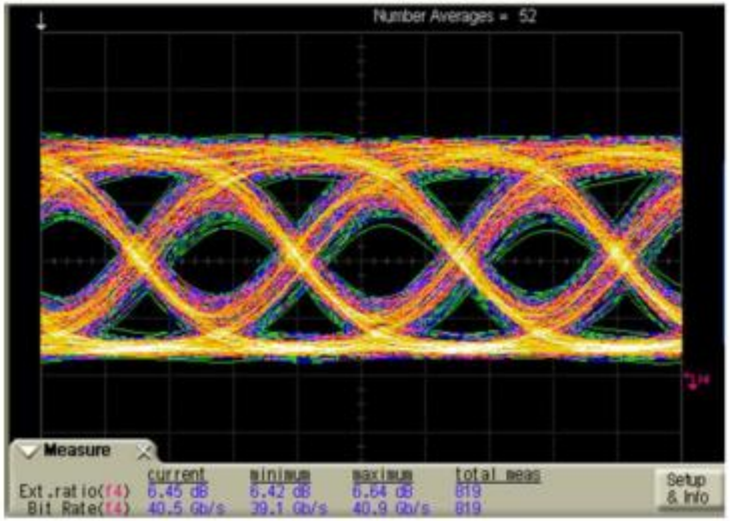
higher radiation level in detectors

Solution A: improve existing option (III-V based components)

Solution B: new technology

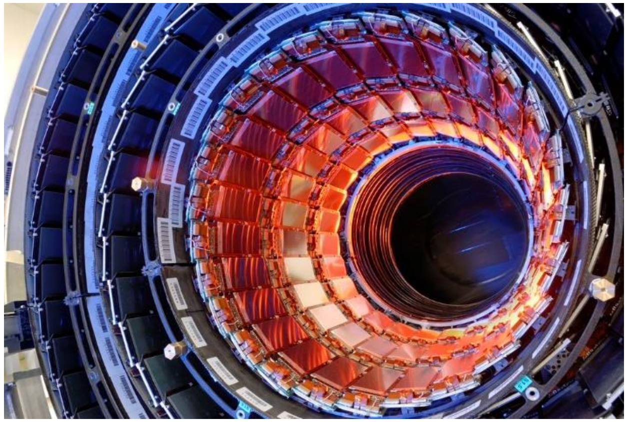
Silicon photonics could be solution B

High data rates possible
➔transmit larger amount of raw data
➔reduce channel count

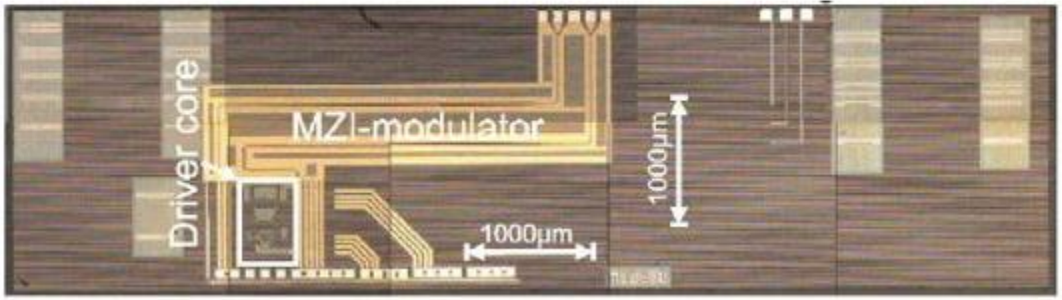


	current	minimum	maximum	total meas
Ext.ratio(f4)	6.45 dB	6.42 dB	6.64 dB	819
Bit Rate(f4)	40.5 Gb/s	39.1 Gb/s	40.9 Gb/s	819

Radiation hardness (CMS's silicon tracker)
➔place transmitters closer to collision center
➔eliminate copper wiring



Possibility for electro-optic integration with driver IC and/or particle sensor
➔less bulk in detector
➔reduce power consumption



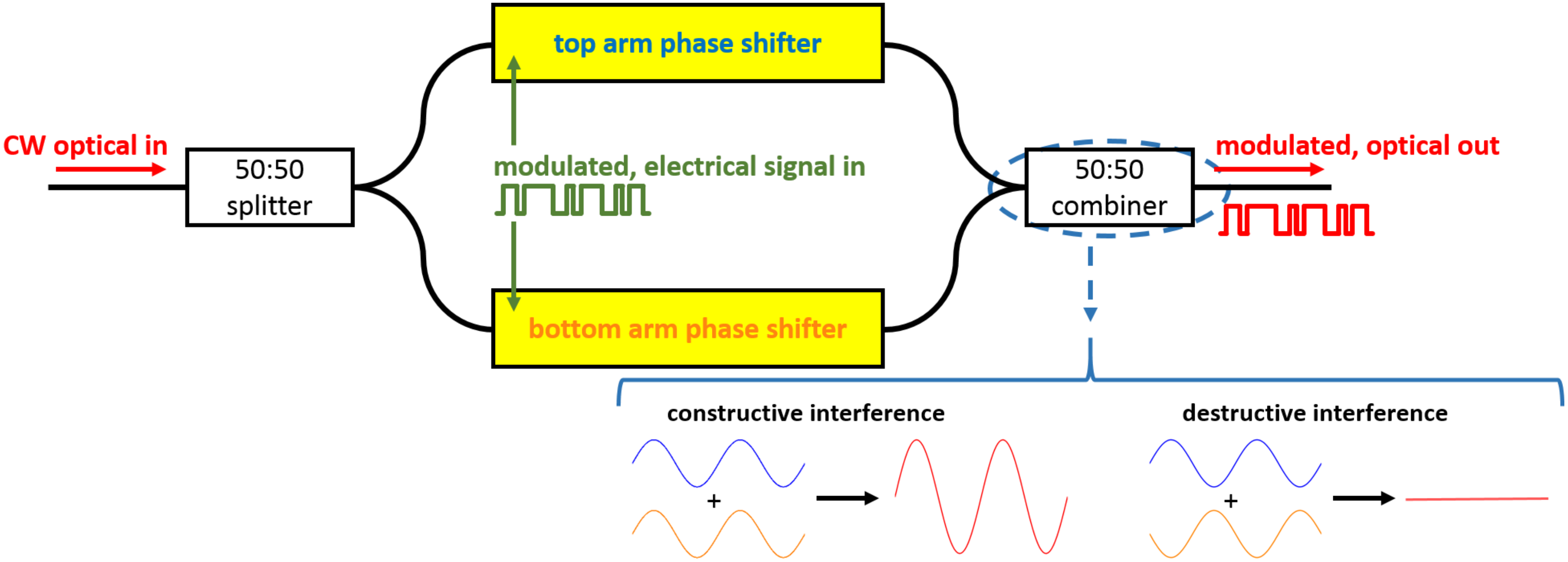
Why do we chose a Mach-Zehnder modulator?

Several possible transmitter technologies in silicon:

- Electro-absorption modulator
    - requires germanium overgrowth, relatively new technology → not fully mature
- Ring modulator
    - high temperature sensitivity → not compliant with requirements
- Mach-Zehnder modulator (MZM)
    - silicon only, wide temperature range, mature technology → best option

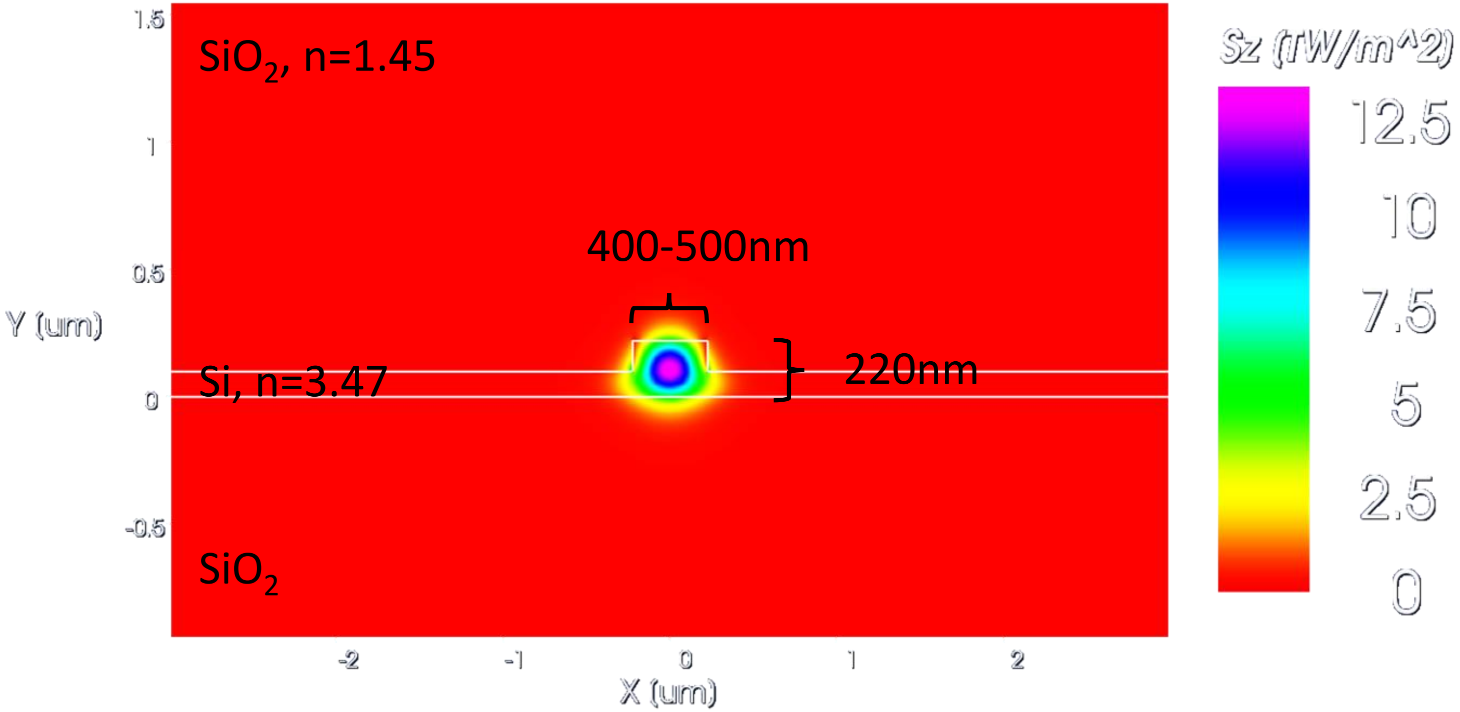
An MZM exploits optical interference to modulate amplitude of light

Phase shift between two interfering light beams causes constructive (1-bit state) or destructive (0-bit state) interference at MZM output



➔ the closer the phase shift to π, the better the optical extinction ratio

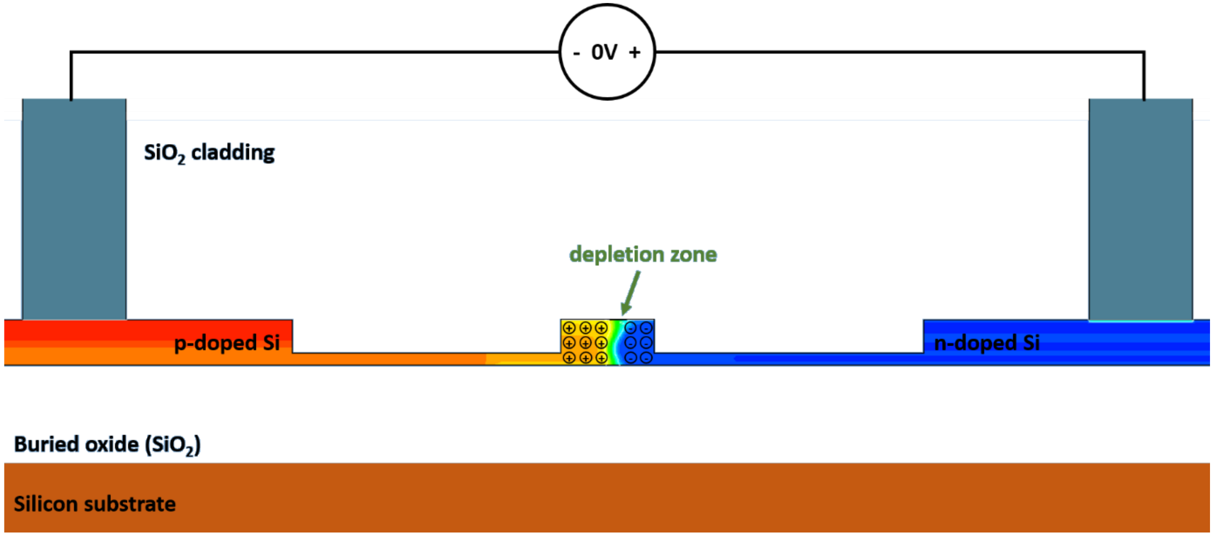
Si/SiO2 waveguides allow very dense integration

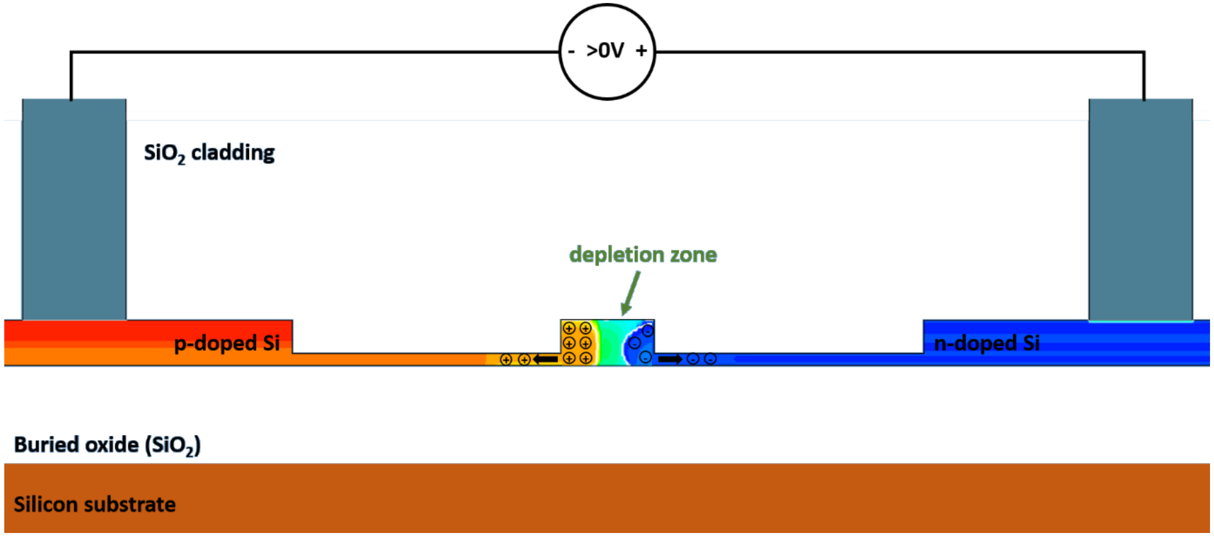


large difference in ref. index leads to strong confinement of light

➔small waveguides, sharp bends possible

How can phase shift be realized? Incorporate a pn-junction into waveguide!





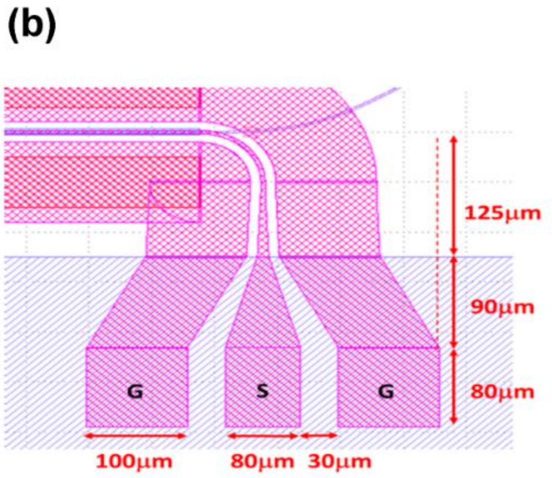
Guided mode interacts with carriers in silicon through plasma dispersion effect:

injection/depletion of carriers changes silicon’s refractive index

↓

refractive index change translates into phase shift

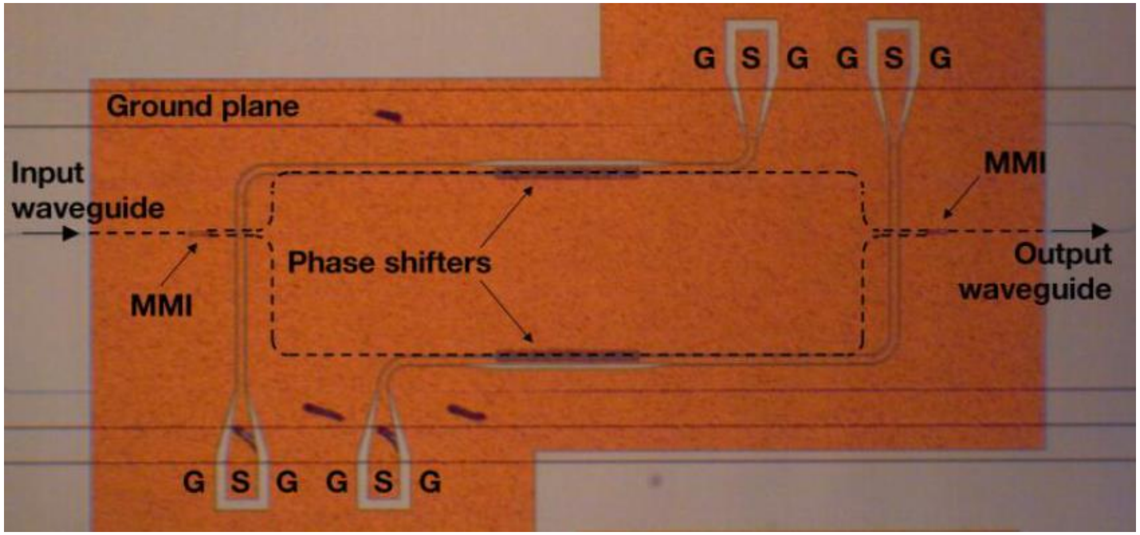
Device that can be fabricated is defined through mask layout



Mask layout:

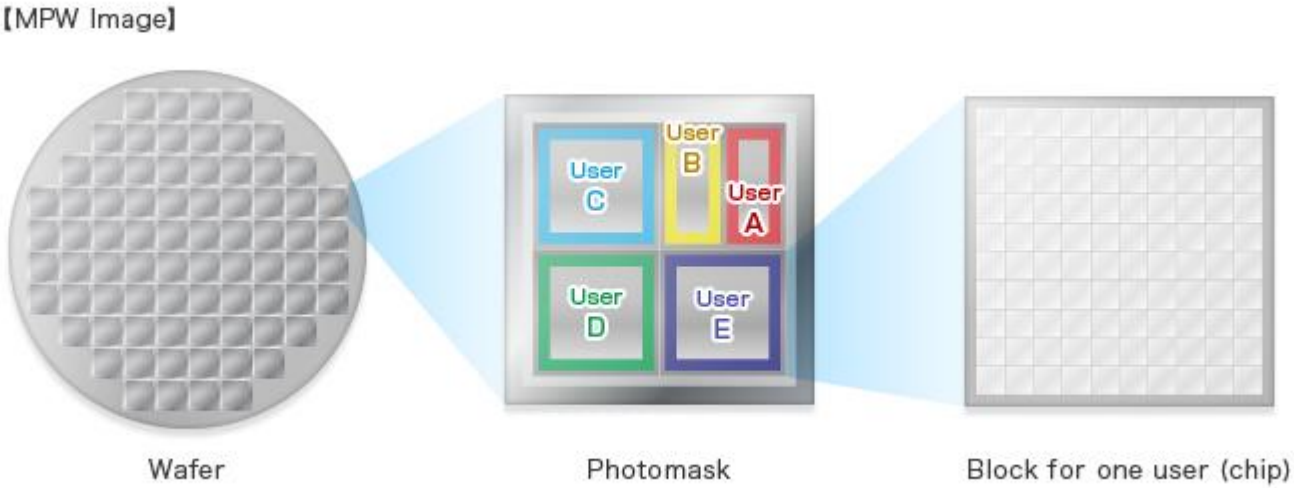
Drawing 2D shapes to define areas where certain fabrication steps are to be done

Fabricated, real device



What is a multi project wafer (MPW) run?

Wafer space and fabrication costs are shared among many different projects (customers)



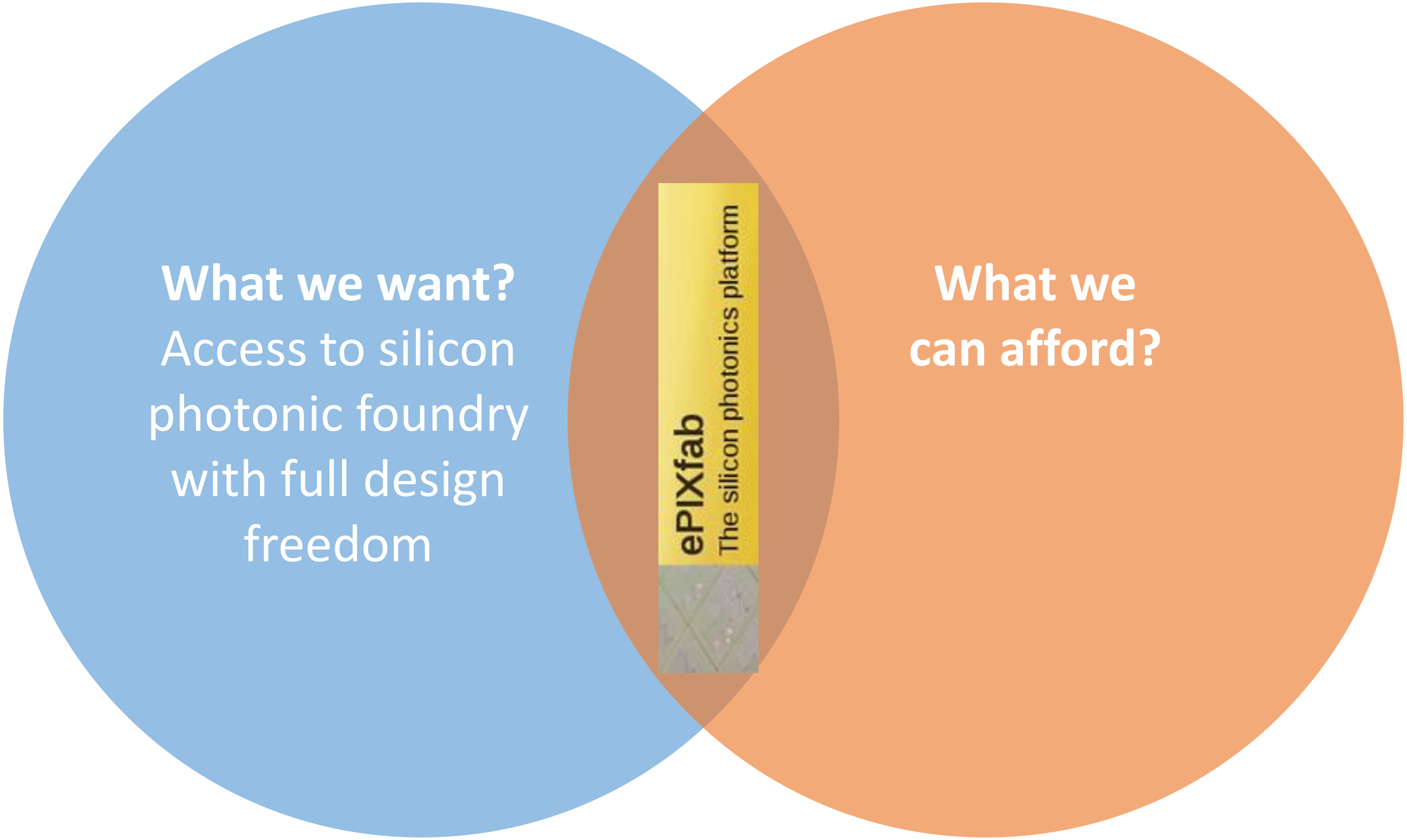
Offered through ePIXfab: consortium of several European silicon foundries

DE LA RECHERCHE À L'INDUSTRIE
cea
leti
imec

innovations
for high
performance
microelectronics

VTT

Biggest advantage: Affordability for Prototyping!

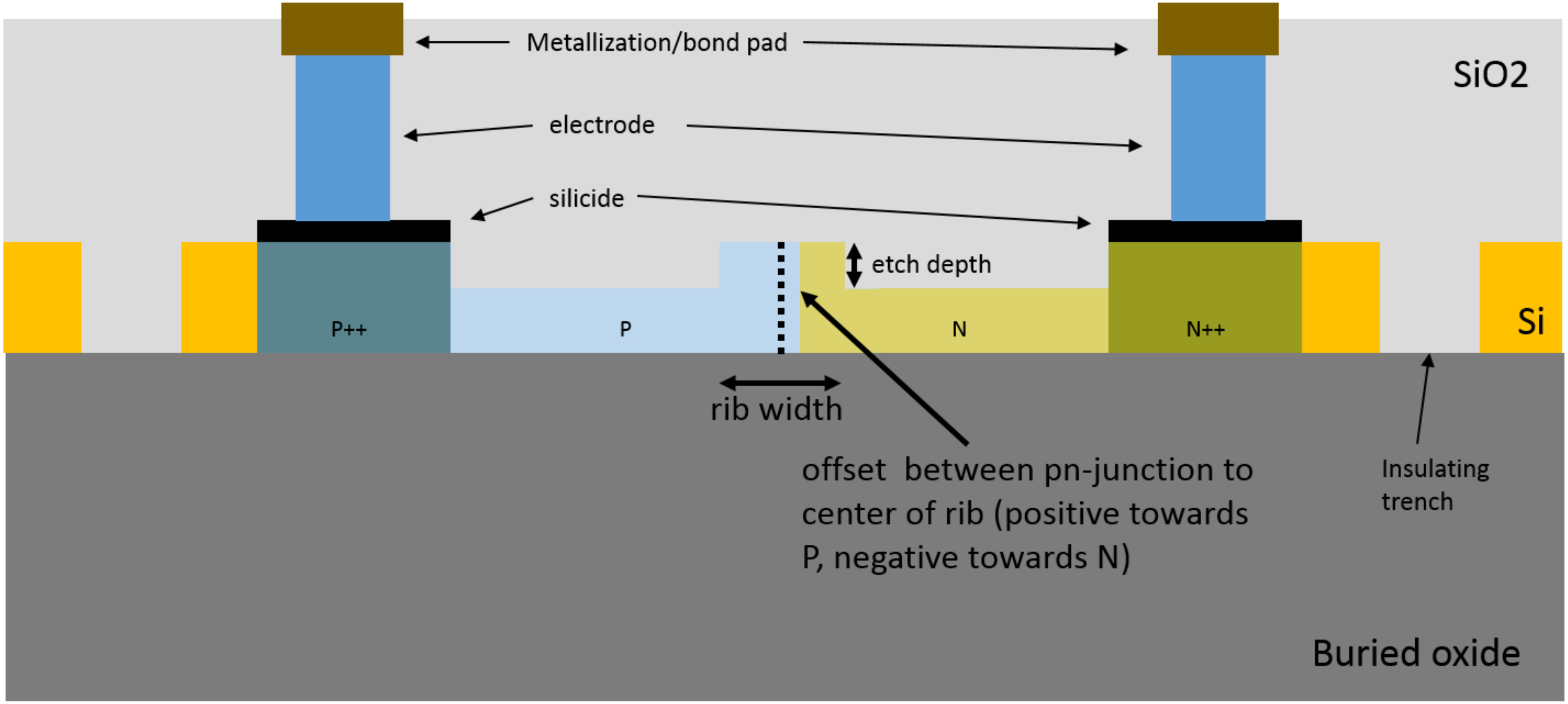


What we want?
Access to silicon photonic foundry with full design freedom

What we can afford?

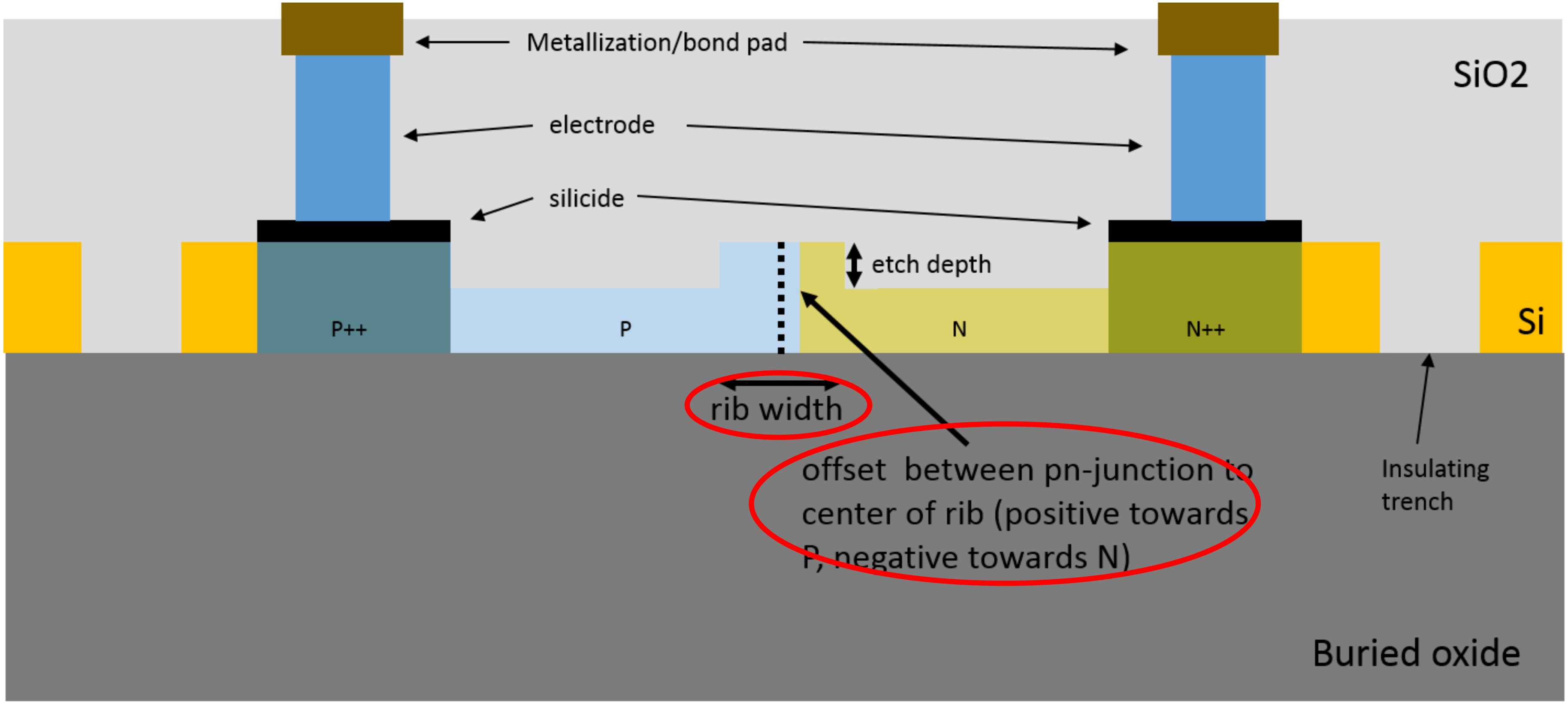
Also:
Availability of pre-designed foundry “building blocks” devices with validated performance
→ lower hurdles for more complicated chip designs

The main restriction is limited design freedom



- Doping not variable: 2 (Leti) or 3 (imec) fixed doping concentrations for n- and p-type
- Fixed etch depth: shallow, deep, full
- Fixed SiO_2 thickness (strong impact on radiation resistance)

But: limited design freedom also means reduced number of possible device designs

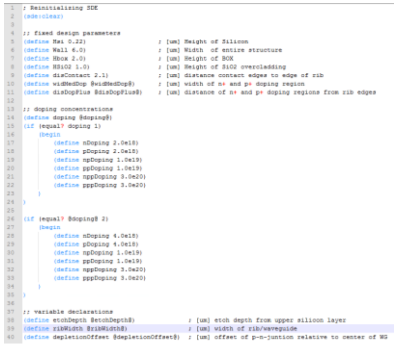


Large phase shift wanted!

➔Best combination of rib width and junction offset for each etch depths must be found before mask layout can be made

Phase shift is predicted with simulations

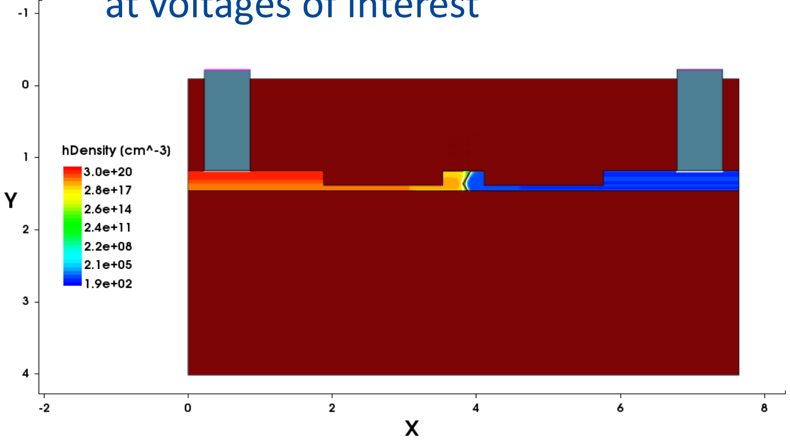
definition of device geometry
for design parameter set of interest



```
; Reinitializing SDE
(sde:clear)

;; fixed design parameters
(define Hsi 0.22)                      ; [um] Height of Silicon
(define Wall 6.0)                      ; [um] Width  of entire structure
(define Hbox 2.0)                      ; [um] Height of BOX
(define HSiO2 1.0)                     ; [um] Height of SiO2 overcladding
(define disContact 2.1)                ; [um] distance contact edges to edge of rib
(define widMedDop @widMedDop@)         ; [um] width of n+ and p+ doping region
(define disDopPlus @disDopPlus@)       ; [um] distance of n+ and p+ doping regions from rib edges

;; doping concentrations
(define doping @doping@)
(if (equal? doping 1)
     (begin
          (define nDoping 2.0e18)
          (define pDoping 2.0e18)
          (define npDoping 1.0e19)
          (define ppDoping 1.0e19)
          (define nppDoping 3.0e20)
          (define pppDoping 3.0e20)
     )
)

(if (equal? @doping@ 2)
     (begin
          (define nDoping 4.0e18)
          (define pDoping 4.0e18)
          (define npDoping 1.0e19)
          (define ppDoping 1.0e19)
          (define nppDoping 3.0e20)
          (define pppDoping 3.0e20)
     )
)

;; variable declarations
(define etchDepth @etchDepth@)                   ; [um] etch depth from upper silicon layer
(define ribWidth @ribWidth@)                     ; [um] width of rib/waveguide
(define depletionOffset @depletionOffset@)  ; [um] offset of p-n-juntion relative to center of WG
```

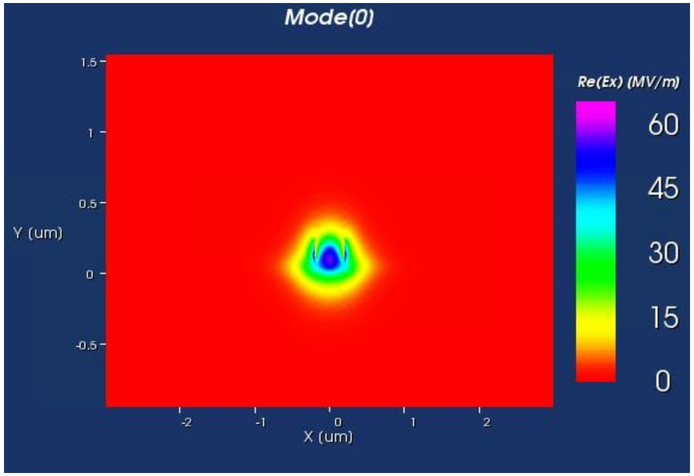
electrical simulation

extraction of carrier densities
at voltages of interest

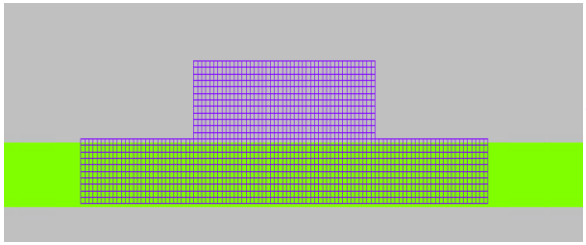


effective refractive index for guided mode at voltages of interest

➔ determines phase shift

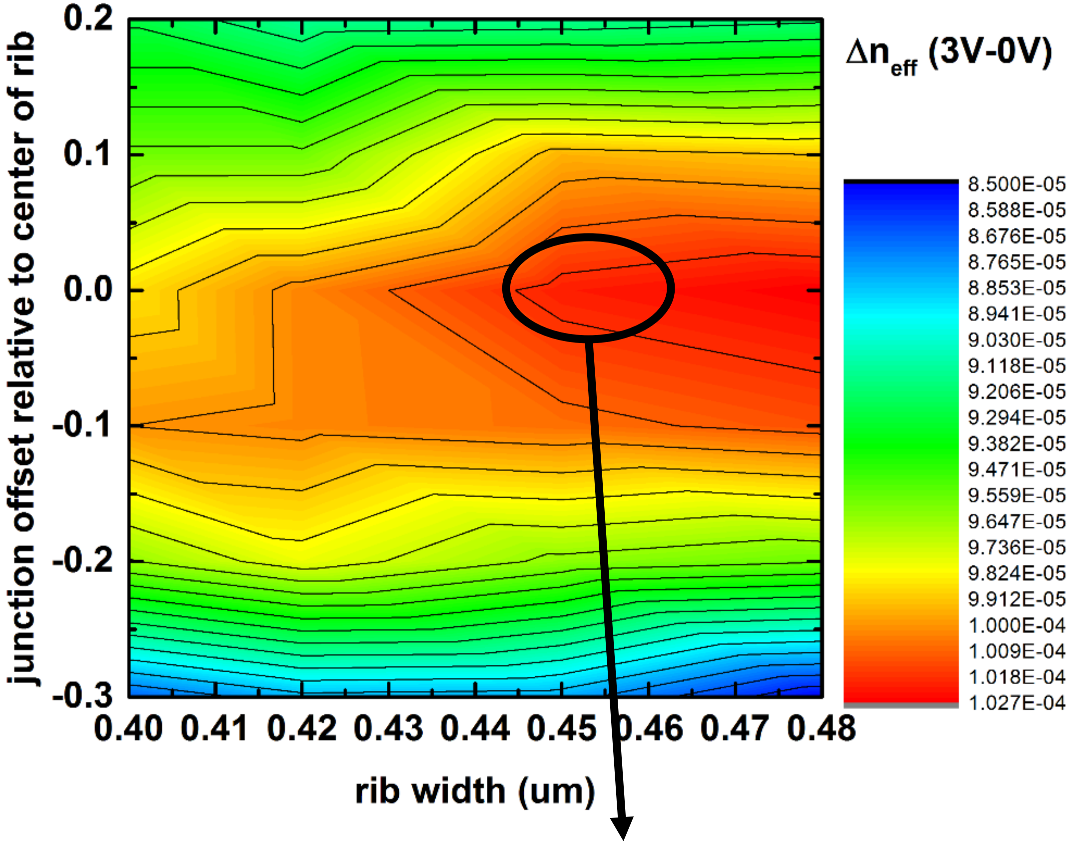


Soref-Benett formula:
carrier density grid to ref. index grid



optical simulation

Example results on the basis of Imec’s shallow etch waveguide



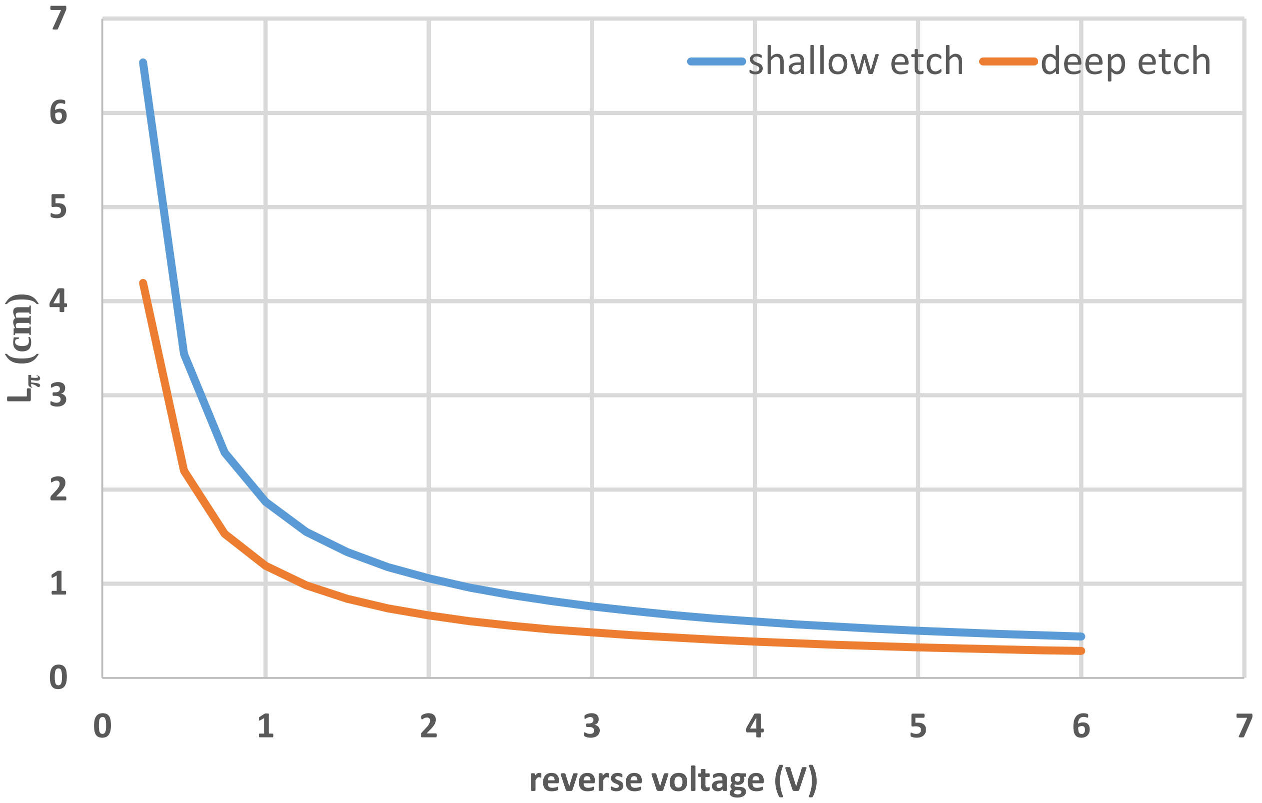
ER=2.25dB

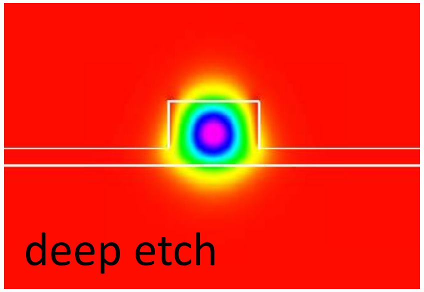
ER=4.99dB

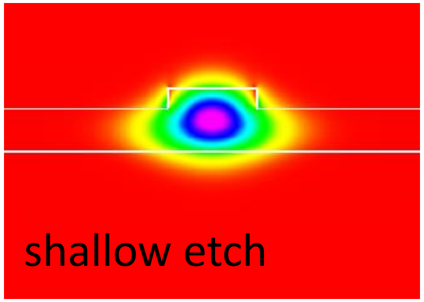
highest change in effective ref. index of guided mode

➔ largest phase shift

Deep etch waveguides show better performance than shallow etch waveguides







Deep etch waveguides have

- larger overlap of depletion zone and optical mode

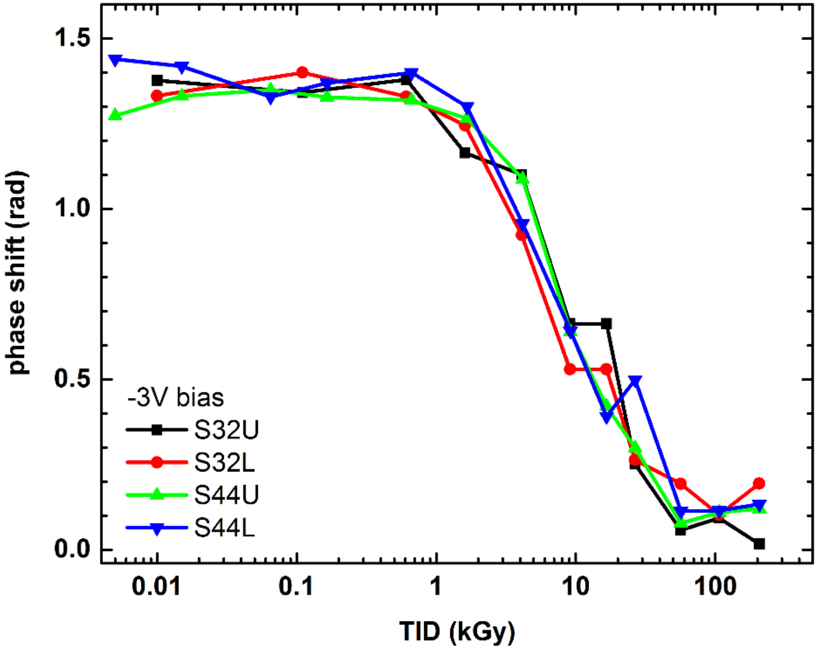
➔higher phase modulation efficiency

➔Shorter phase shifter length for π phase shift required

Radiation effects are not included in simulations

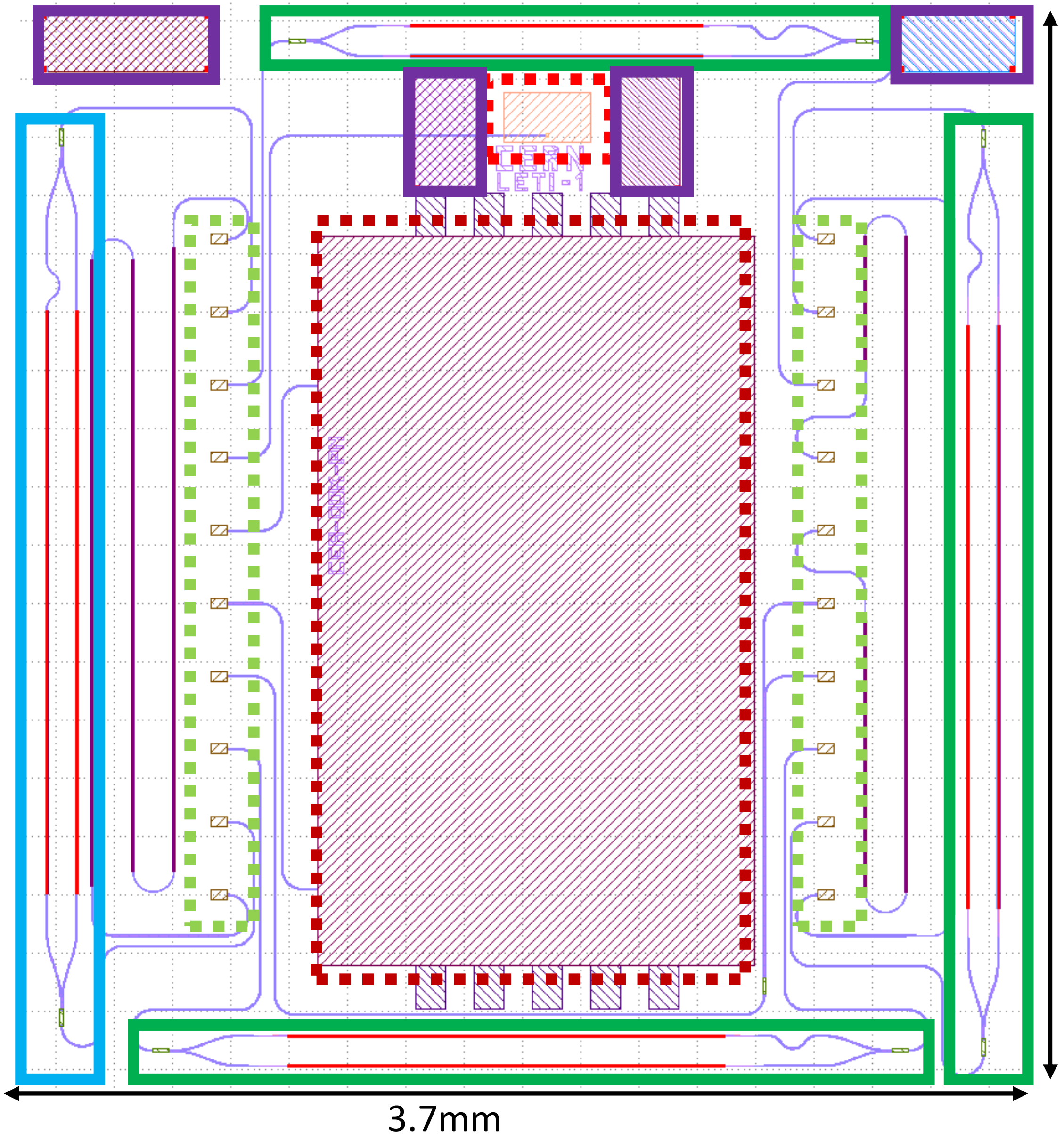
Previous experiments show phase shift degradation with increasing x-ray dose

But: No quantitative simulations to predict radiation response of devices found yet.



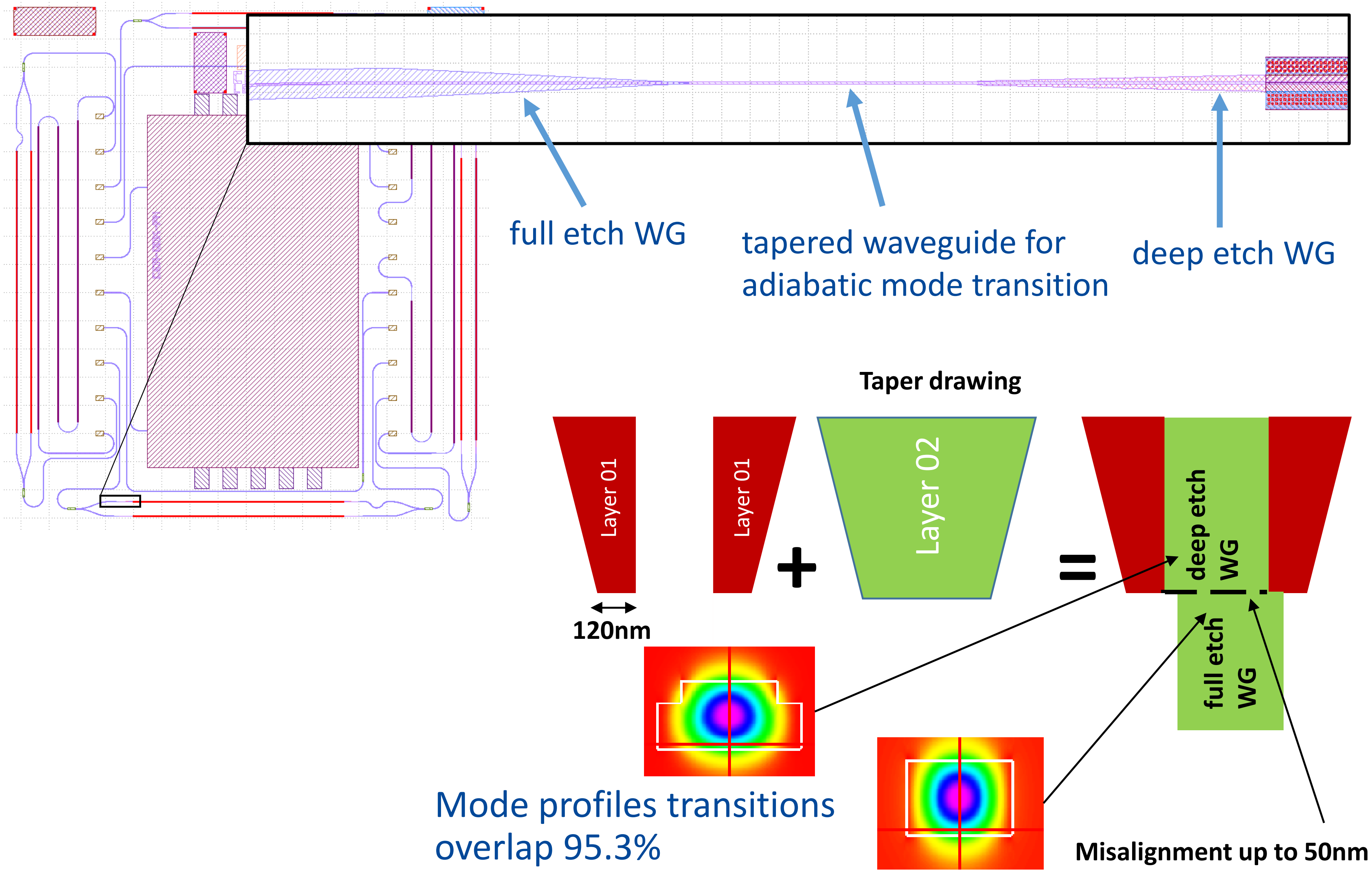
Assessment of radiation hardness as function of dose and device design has to be done experimentally!

What is actually included in Leti chip layout?



- 1 Leti building block MZM
- 1 Leti building block photo diode
- 20 Leti building block grating couplers as optical input/output
- 3 deep etch custom design MZMs with different lengths
- 1 shallow etch custom design MZMs with different lengths
- 4 doped regions for material analysis

Connection of Leti building block to custom design required taper



full etch WG

tapered waveguide for adiabatic mode transition

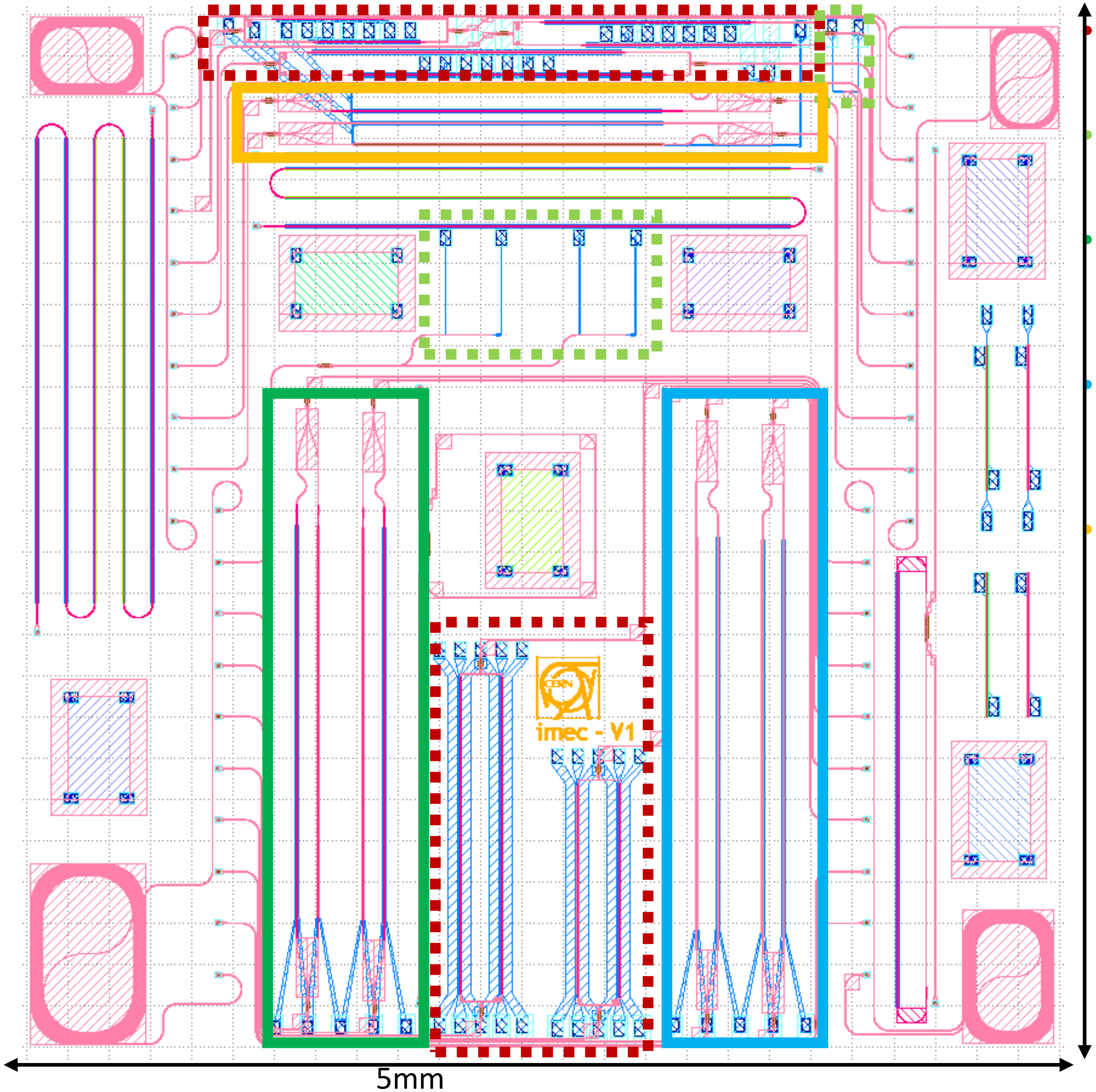
deep etch WG

Taper drawing

Mode profiles transitions overlap 95.3%

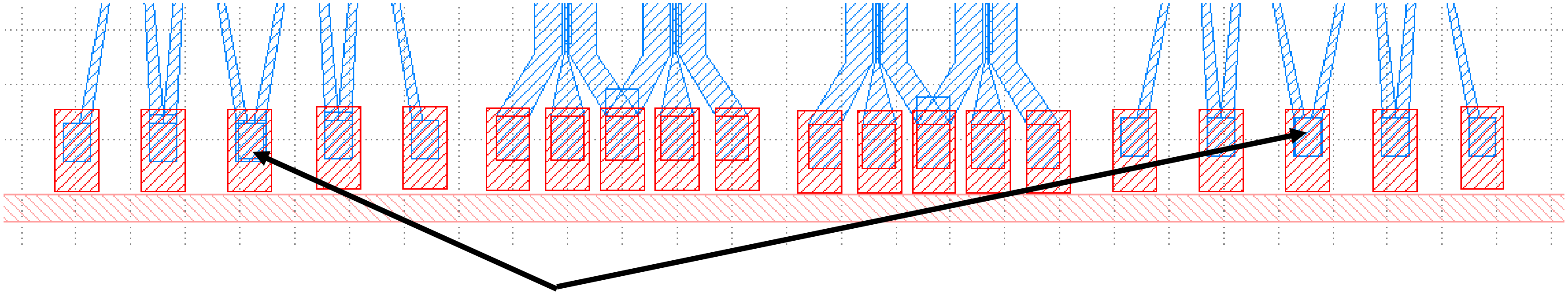
Misalignment up to 50nm

There are more active components on Imec layout

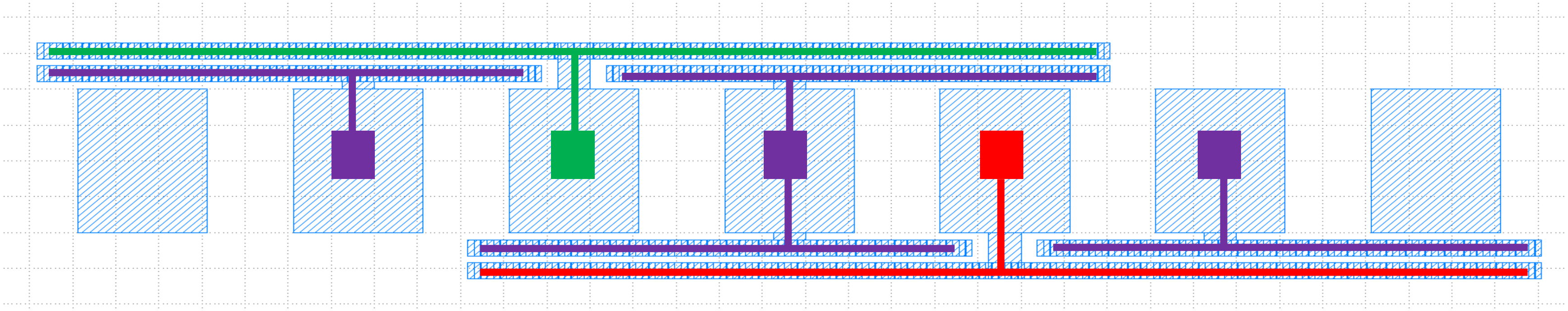


- 6 Imec building block MZMs with different parameter sets
- 3 Imec building block photo diodes
- 2 deep etch custom design MZM for 1550nm with different doping widths
- 2 shallow etch custom design MZMs for 1550nm with different doping widths
- 1 deep and 1 shallow etch custom design MZM for 1310nm

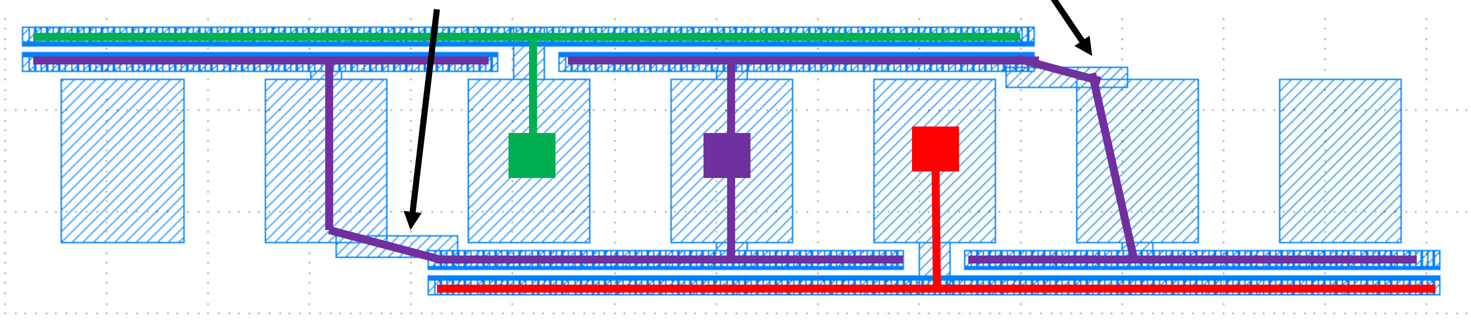
Initial space for bond pads for active devices was not enough



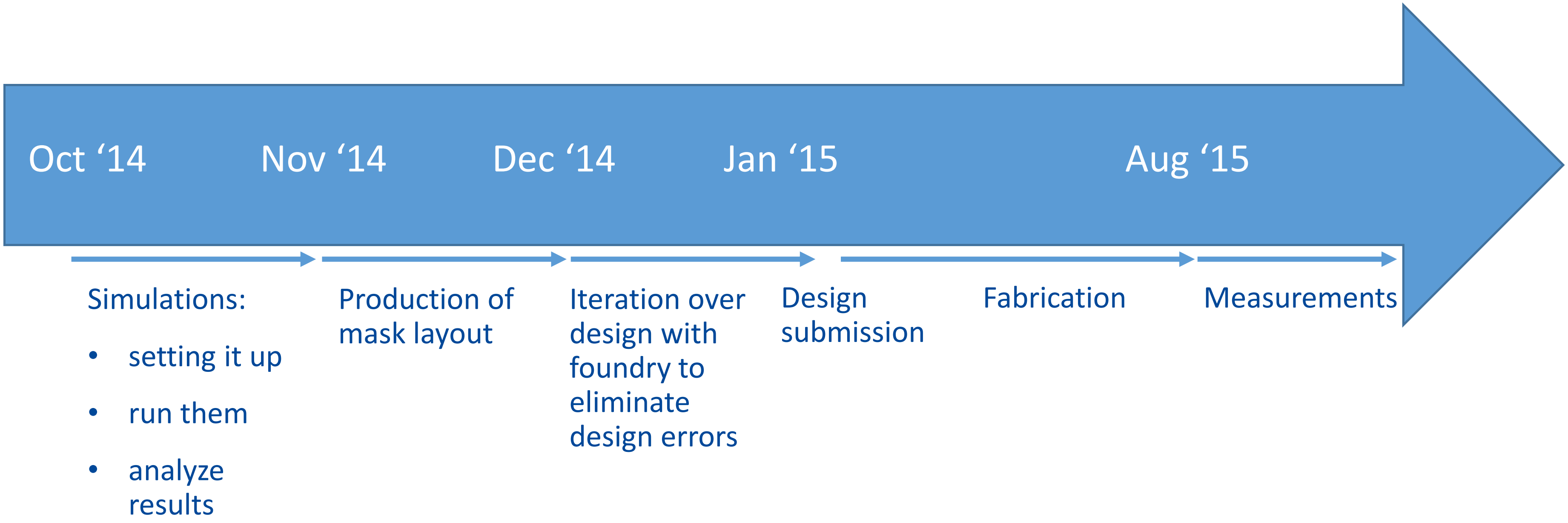
custom MZMs share one signal bond pad



added shorts to reduce number of bond pads for building blocks



How long does everything take?



Oct ‘14

Nov ‘14

Dec ‘14

Jan ‘15

Aug ‘15

Simulations:

- setting it up
- run them
- analyze results

Production of mask layout

Iteration over design with foundry to eliminate design errors

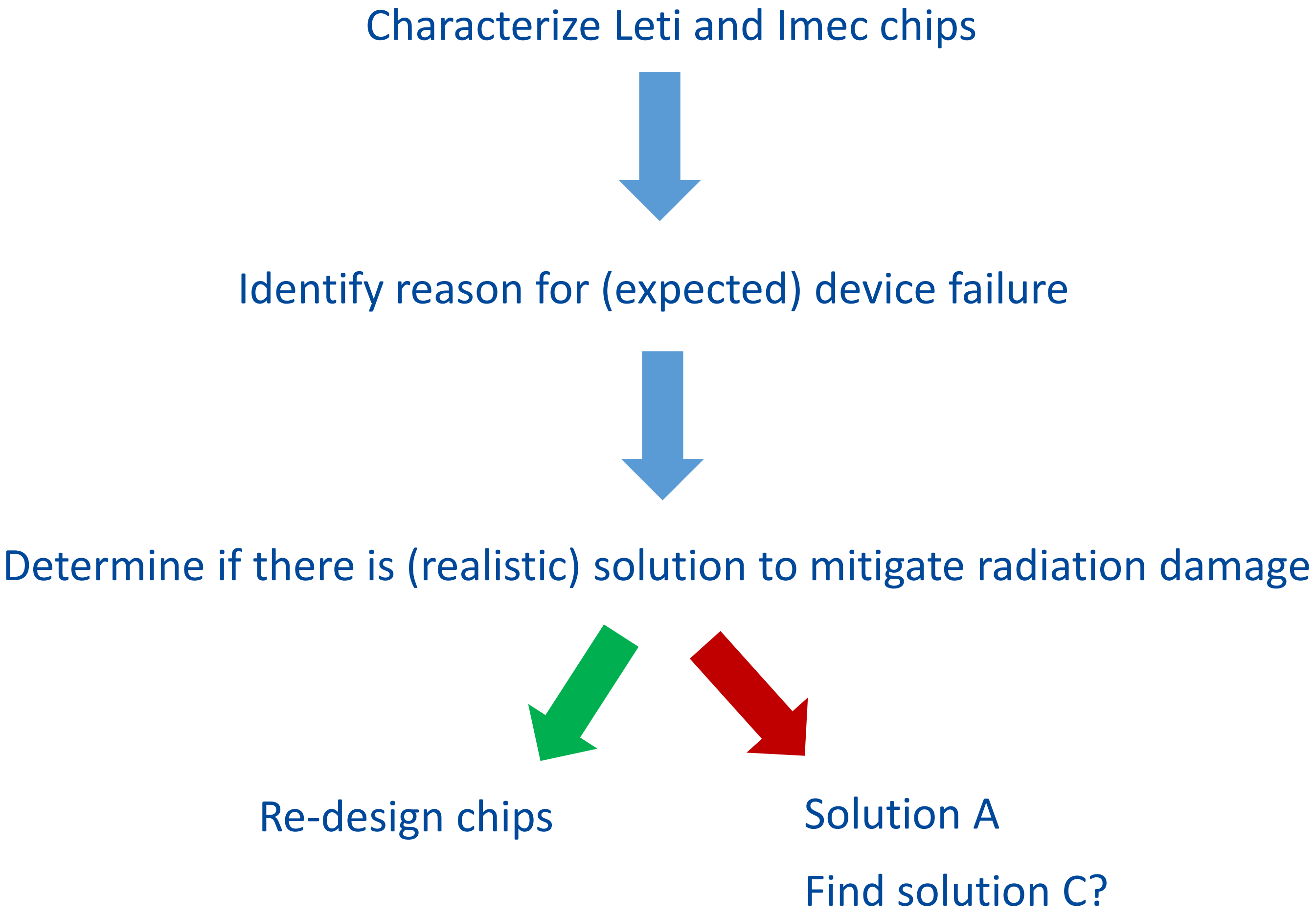
Design submission

Fabrication

Measurements

What comes next?

Question “Can CERN benefit from SiPh technology?” needs to be answered.



Characterize Leti and Imec chips

Identify reason for (expected) device failure

Determine if there is (realistic) solution to mitigate radiation damage

Re-design chips

Solution A

Find solution C?