Tools and scalability at openlab CERN **Andrzej Nowak** openlab June 21st 2010

2nd Workshop on adapting applications and computing services to multi-core and virtualization CERN





> Architecture outlook and performance

> Shifts in performance tuning

> Tools used for performance optimization

- Platform usage efficiency
 - perfmon2
 - VTune and PTU
 - Piersol HE (upcoming)
- Threading performance
 - Thread profiler
 - Piersol HE (upcoming)
- Correctness
 - Thread Checker
 - Cantua HE (upcoming)



Architecture outlook

> Current Intel microarchitecture: "Westmere"

- 32nm, Nehalem based
- Up to 6 cores per chip, we use 2 sockets: 24 threads

> Current Intel multiprocessor architecture: "Beckton"

- 45nm, Nehalem-EX
- Up to 8 cores per chip, up to 8 sockets per platform: 128 threads

> Forthcoming developments:

- 2010/2011: "Sandy Bridge" 256 bit SSE (AVX), 8 cores
- 2011/2012: "Ivy Bridge" shrink to 22nm
- 2012/2013: "Haswell" possible uarch redesign, further integration, FMA



Architecture and platform performance (1)

- > Openlab tested a Westmere-EP system and a Nehalem-EX system: papers available at <u>http://cern.ch/openlab</u>
- > Westmere-EP (12 cores)
 - 50% core increase, but HEPSPEC06 numbers only 32% better
 - Core Clock-per-clock throughput comparison very close to Nehalem
 - Overall improvements between 39% and 61% (mostly due to core increase) wrt Nehalem
 - SMT benefit mostly unchanged, 10-23% performance per Watt improvement
 - Some multi-core effects inhibit scalability



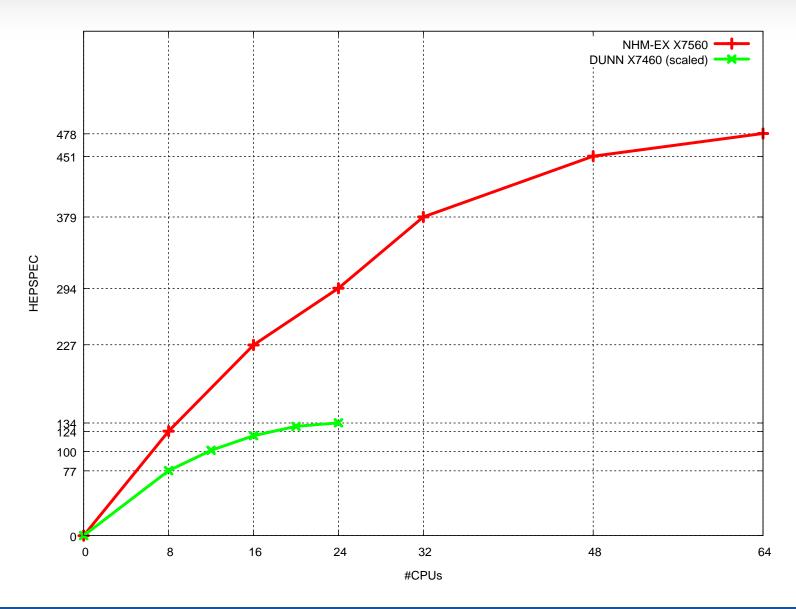
Architecture and platform performance (2)

> Nehalem-EX (32 cores)

- 33% core increase reflected in performance
- 29.7x speedup obtained with a multi-threaded Geant4 prototype (FullCMS simulation) compared to 1 thread
 - Minor memory usage per thread
- "Top of the line" CPU comparison w/ Dunnington (24 cores), unscaled
 - 3x more throughput on HEPSPEC06
 - 11%-60% more throughput elsewhere
- SMT advantage: 19%-28%
 - More than expected; might be related to the fact that SW doesn't scale well to 32 cores
- Significant power consumption
- Some multi-core effects inhibit scalability scalability lines on graphs should be straight, but are not



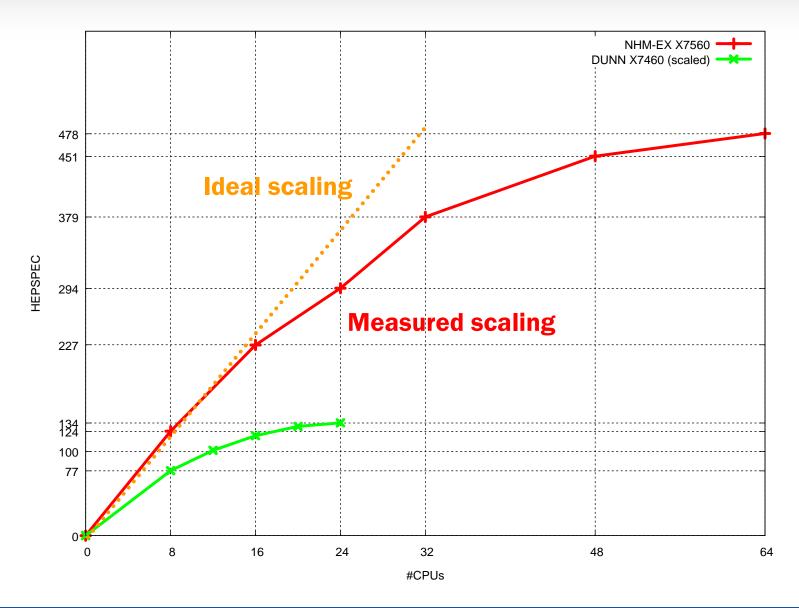
Nehalem-EX – HEPSPEC06 curve



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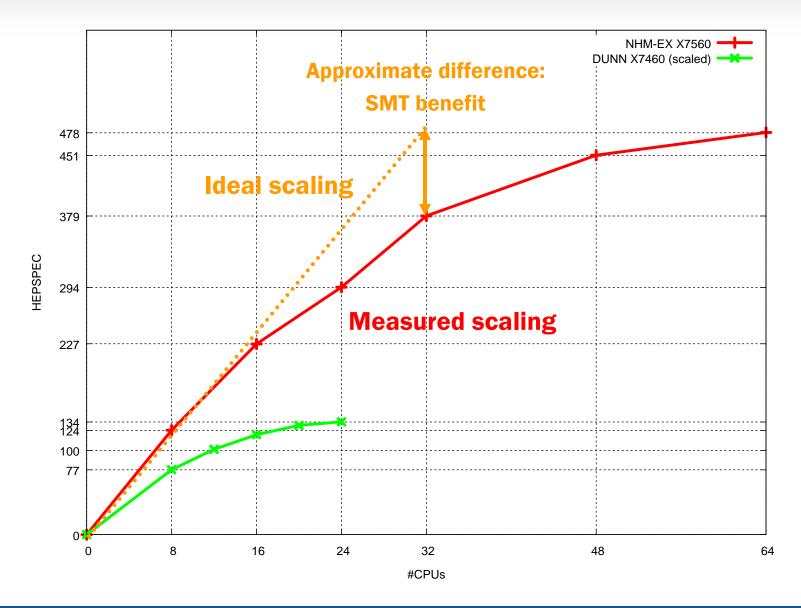
Nehalem-EX – HEPSPEC06 curve



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Nehalem-EX – HEPSPEC06 curve



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Mainstream architecture and platform trends

> Core development:

- X86-64 remains the architecture of choice
- Continued <u>incremental</u> core increase
 - Decreasing relative cache advantage: smaller size, larger distances, increased penalty risk, lower predictability
- Added functional units
 - i.e. Crypto, AVX, FMA, Graphics
- 4-way hardware threading unlikely on OOO

> Platform development:

- Many-core scaling effects already noticeable
- NUMA effects already noticeable large impact on multi-threading and SHM-based software, impact on multi-processing
- Increasing memory demand and pressure
 - More memory capacity expected (increasing part of the cost and power!)
 - More memory levels
 - More system memory does not guarantee more bandwidth, throughput or performance
- DP likely to remain the platform of choice and develop well for the next several years – market "sweet spot"
 - Pricing on more developed systems is prohibitive





Sood news:

- Our window onto the hardware (performance counters) is being improved and systematized
 - The importance of hardware counters has been understood by the industry
 - openlab has direct links to HW/SW architects and other key people
- Counter-level software becoming more widespread, growing adoption and understanding in the HEP community
- Software is becoming more robust and accessible (i.e. GUIs)

> Bad news:

- The complexity of performance analysis is growing
 - Architecture complexity is increasing (i.e. NUMA)
 - Language complexity is increasing (C++, Java proliferation)
 - It's harder to implement the tools because of the above and because of the increased complexity of the environment (kernel, etc)
- And it was already hard in the first place
- > Where Linux "PCL" will miss, private companies (like Intel) will hit
- > Hardware counters can be used to measure I/O, but it's hard





> A Linux interface to the performance monitoring counters

Supports counting, flat profiles and sampling in intervals

> Pros:

- Lightweight, robust and open source
- Long running project with extensive experience
- Relatively stable and reliable, even with HEP software (in part thanks to efforts at openlab)
- Easy to modify, easy to use to instrument HEP code (see CMS)
- Direct link with the main architect

> Cons:

- SLC-based kernel is provided in binary form, but is not standard SLC
- Limited analytical capabilities in the package:
 - counting, flat profiles, sampling in intervals
- Little hopes of further extensive development "PCL" hijacked the functionality (far from being ready)



perfmon2 – obtaining and using

> Restrictions:

- Kernel is modified SLC based config but different version
- Superuser access needed for installation
- > Profiles available for managed SLC5
- > RPMs available for manual installation on SLC5
- > Manual installation: complicated but possible
- > Successfully used at CERN in many contexts
 - Extensive monitoring in the computing center
 - Framework analysis and debugging
 - Snippet analysis
 - CMS instrumentation

> All resources:

twiki.cern.ch/twiki/bin/view/Openlab/Perfmon2

VTune and PTU



> PTU – "VTune on steroids"

- The tool of choice of a performance monitoring expert
- Supports counting, profiles, comparisons, memory profiling, call graphs (statistical and instrumentation based), basic block analysis, call count
- Supports graphing: Events over time, events over IP, Memory traffic (heap profiler, data access profiling)
- > Pros:
 - Very robust tool with a variety of analytical capabilities
 - Code instrumentation possible
 - Does not need a special kernel, works fine with SLC5
 - Direct link with the main architect (coming to CERN in July)

> Cons:

- Might be too sophisticated for occasional users
- Proprietary license needed (although we have plenty at CERN)
 - Free support and <u>discounted/free licenses</u> for academic institutions
- No source, modifications impossible
- Official support very limited
- Stability with HEP software sometimes leaves room for improvement
 - To be fixed in an upcoming future version 4.0

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Intel(R) Performance Tuning Utility - /root/workspace/mtg4/Loop-Analysis-2010-05-10-13-15-22 - Eclipse Platform

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PTU – obtaining and using

> Practical restrictions:

- Superuser access needed for installation
- Works best with the GUI, command line obscure
- Rather sluggish there are some overheads which are still being investigated

> Obtaining PTU:

- Download from the Intel website
- Source the license file in your shell as described here:
 - twiki.cern.ch/twiki/bin/view/Openlab/IntelTools
- Install PTU by running the installer
- Run script to compile and install the kernel driver

> Running:

- Use GUI or refer to user guide for numerous command line options
- > Successfully used at CERN for several projects
 - Framework and snippet analysis and debugging
 - CMS monitoring and source annotation
 - ATLAS, Geant4 monitoring and analysis



> A promising next-generation performance monitoring tool from Intel

- A fusion of PTU and Thread Profiler, will support threaded profiling
- Simplified and modernized GUI, without sacrificing functionality
- Several levels of analysis depth available
 - Many PIN-based engines (http://pintool.org)
- Linux native
- Kernel driver will be needed (but no kernel change required)
- More in H2 2010 possible workshops



Threading performance – Thread Profiler

> Thread Profiler from Intel

- Bottleneck analysis
- Synchronization issues
- Locates inefficiencies and sub-optimal resource usage

> Visual representation of threading performance issues

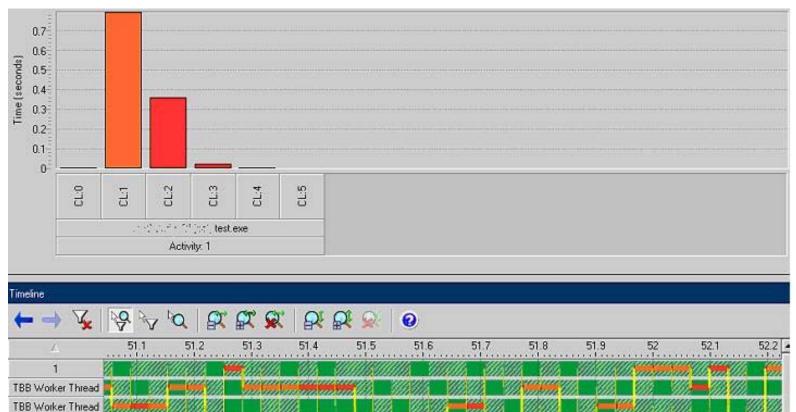
- Concurrency and thread state graph ("profile view")
 - Different breakdowns available
- Transitions graph and timeline ("timeline view")
- Supports OpenMP and pthreads (and Windows API threads)
- **>** Source instrumentation and binary instrumentation
- > Remote data collection possible
- > Used successfully for debugging prototype multithreaded applications at CERN



Thread profiler – view

> Dark green = good work, light green = no work, waiting, idle

- > Orange/red critical path
- > Yellow transitions

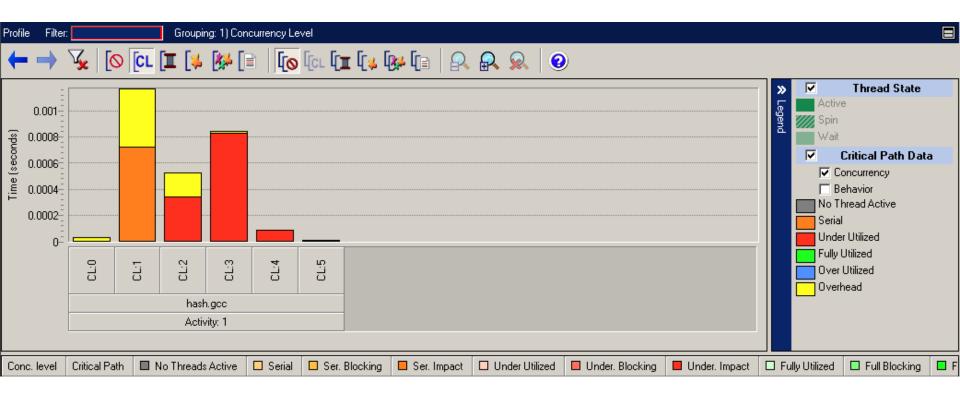


TBB Worker Thread



Thread profiler – profiler view

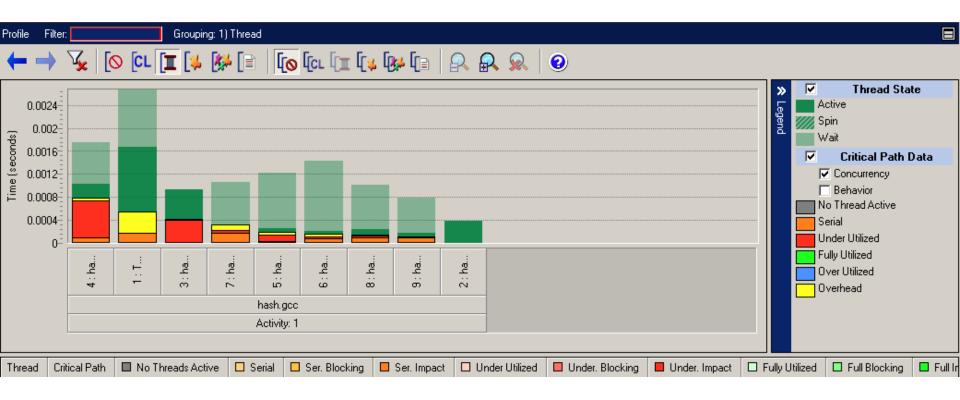
>Concurrency level grouping





Thread profiler – profiler view

>Thread grouping

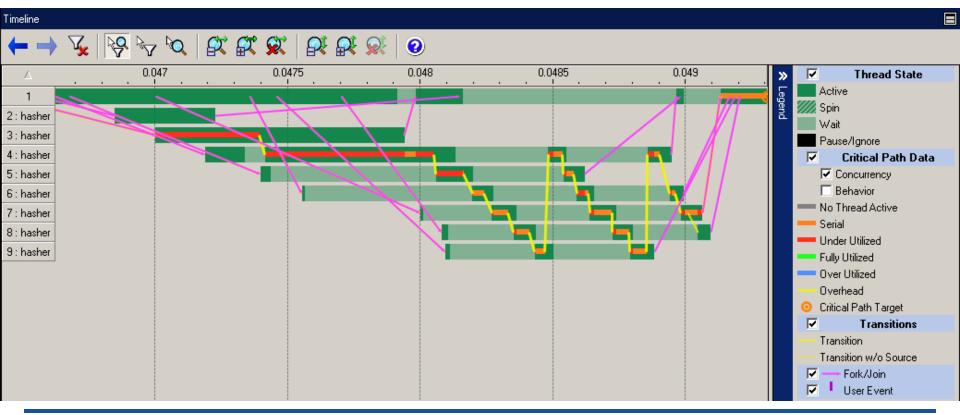




Thread profiler – timeline view

>Critical path display

>Light green portions show wait time, dark green show work



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Thread Profiler - typical workflow

1. Collect on Linux

- Either compile with -tprofile or openmp_profile (source instrumentation - better option)
- Or just run tprofile_cl yourprogram (binary instrumentation)
- **2.** Copy bistro/.tp output files over to Windows and analyze in the GUI



Checking for correctness

>Intel Thread Checker

- Rather old tool with interesting capabilities
- Anomaly detection: Deadlocks, Stalls, API usage violations, Race conditions, Memory overwrites, Abandoned locks

> Data analysis:

- Data collection and text analysis in Linux
- The trace file can later be opened in the Windows version of the tool for detailed analysis

Thread Checker screenshot



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Thread Checker – typical workflow

1. Collect on Linux

- Either compile with -tcheck (source instrumentation better option)
- Or just run tcheck_cl yourprogram (binary instrumentation)

2. Analyze

- 1. Either directly use the text output produced by the program
- Or copy files over to Windows and analyze in the GUI (more information available, "clickable" source)



Upcoming tool from Intel: Inspector

> Next-generation correctness checking tool from Intel

- Threading support: pthread, OpenMP, TBB
- Detects race conditions, memory conflicts, locking conflicts and other issues
- Robust memory correctness checker

> Several levels of analysis depth available

- Many PIN-based engines (http://pintool.org)
- > Linux native
- > No kernel driver needed, no privileges needed
- > Successfully tested at openlab, feedback provided
 - ROOT
 - Geant4
- > Public beta in H2 2010

		Inters Cantua HE Checker - New Cantua HE Checker Result	
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🔁 📓 Memory Er	rrors 💽 😰 🕕		
r006mi r003ti	New Cantua HE Checker Result 🗷		

Configure Tar	get and Analysis Type		Intel's Cantua HE checke
🖲 Target 🔺 Analysis	: Туре		
A Memory Errors A Threading Errors Custom Analysis Ty	Memory Errors Choose a preset configuration designed to h custom configuration using another configur	elp you control analysis cost (duration). You can fine-tune a preset configuration or create a ration as a template.	Analyze Stop Take snapshot
	Analysis scope: Medium Detect resource leaks: Yes Stack frame depth: 12		
	,	Yes Yes Yes No No 1 Mb No 32 bytes 12	

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🔁 📔 Memory Errors - 🛛 😂 🕕

r006mi 🗵

📒 Memory Errors

Summary & Details

Obse	rva	ations							?
ID	۹	Description	Problem	Source	Function	Mod	Object	State	-
X5556	۲	Allocation	Memory leak	🖻 vector.tcc:357	_M_fill_insert	test40	32	▶ Not fi	
X5557	۲	Allocation	Memory leak	🖻 vector.tcc:357	_M_fill_insert	test40	32	🎙 Not fi	
X5558	۲	Allocation	Memory leak	vector.tcc:357	_M_fill_insert	test40	32	🎙 Not fi	
X5559	۲	Allocation	Memory leak	🖻 vector.tcc:357	_M_fill_insert	test40	32	🎙 Not fi	
X5560	۲	Allocation	Memory leak	🖻 vector.tcc:357	_M_fill_insert	test40	32	🎙 Not fi	
X556	۲	Allocation	Memory leak	vector.tcc:357	_M_fill_insert	test40	32	▶ Not fi	
X5562	۲	Allocation	Memory leak	🖻 vector.tcc:357	_M_fill_insert	test40	32	🎙 Not fi	
X5563	۲	Allocation	Memory leak	🖻 vector.tcc:357	_M_fill_insert	test40	32	🎙 Not fi	
X5564	۲	Allocation	Memory leak	vector.tcc:357	_M_fill_insert	test40	32	▶ Not fi	
X5565	۲	Allocation	Memory leak	vector.tcc:357	_M_fill_insert	test40	32	🎙 Not fi	
X5566	۲	Allocation	Memory leak	🗈 vector.tcc:357	_M_fill_insert	test40	32	🎙 Not fi	
X5567	۲	Allocation	Memory leak	🖻 vector.tcc:357	_M_fill_insert	test40	32	🎙 Not fi	
X5568	۲	Allocation	Memory leak	vector.tcc:357	_M_fill_insert	test40	32	🎙 Not fi	
X5569	۲	Allocation	Memory leak	🖻 vector.tcc:357	_M_fill_insert	test40	32	🎙 Not fi	
X5570	۲	Allocation	Memory leak	🗈 vector.tcc:357	_M_fill_insert	test40	32	Not fi	
X557	۲	Allocation	Memory leak	vector.tcc:357	_M_fill_insert	test40	32	▶ Not fi	

Intel's Cantua HE Checker - r006mi

Me	emor	ry leak: Obser	vations in Prob	lem Set					Observations / Timelin	e ?
ID		Description 🔺	Source	Function	Module	Object Size	State	Offset		
∀X 5	566	Allocation site	vector.tcc:357	_M_fill_insert	test40	32	Not fixed			
	355 356	_len = thi	s->max_size();							
-	357	iterator	_new_start(this->	_M_allocate(len));					
-	358	iterator	new_finish(new	w_start);						
3	359	try								

Summaries/Subsets	Sort + X
🗂 Severity	
Error	33381 it
Description	
Allocation site	33226 it
Read	155 items
Problem	
Invalid memory access	4 items
Memory leak	33221 it
Uninitialized memory access	156 items
Source	
DetectorConstruction.cc	650 items
enginelDulong.cc	27 items
G4AllocatorPool.cc	470 items
G4Alpha.cc	1 item
G4AntiBMesonZero.cc	1 item
G4AntiBsMesonZero.cc	1 item
G4AntiDMesonZero.cc	1 item
G4AntiKaonZero.cc	1 item
G4AntiLambda.cc	1 item
G4AntiLambdacPlus.cc	1 item
✓ more	
Function	
cxa_atexit	1 item
libc_start_main	2 items
_M_fill_insert	625 items
_M_insert_aux	1393 ite
AddData	104 items
AddElement	156 items
AddElementByWeightFraction	26 items
AddEmModel	780 items
AddMaterial	95 items
AddRootLogicalVolume	13 items
✓ more	
Module	
test40	33381 it
State	

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Intel's Cantua HE checker

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		Intel's Cantua HE Checker - New Cantua HE Checker Result	
<u>F</u> ile Inspect Help			
📔 📓 Memory Errors	 ✓ 😂 Φ 		
r006mi r003ti New	Cantua HE Checker Result 🗷		
📕 Configure Ta	rget and Analysis Type		
🛛 \varTheta Target Å Analysi	s Туре		
A Memory Errors	Threading Errors		
A Threading Errors	Choose a preset configuration des	igned to help you control analysis cost (duration). You can	fine-tune a preset configuration or create a

Custom Analysis Ty custom configuration using another configuration as a template.

Analysis scope:	Very wide	•
Terminate on deadlock:	No	•
Stack frame depth:	12 🗘	
┌		
runtc SettingsDetect lock hierarchyTerminate on deadlocDetect potential privaStack frame depth:Detect data races:Memory access byte	:k: ac y infringements:	Yes No Yes 12 Yes 1 byte
Detect data races on	stack accesses:	Yes

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Intel's Cantua HE checker

& Analyze

🗢 Take snapshot)

Stop

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<u>F</u> ile Ins	spect Help									
🛛 🖾 🕅	Memory Errors	s 🔹 🖬 📾								
	r003ti 🗷									
									ntel's Cantua HE checker	
Threading Errors										
Summary # Details										
Problem Sets							Summaries/Subsets	Sort • * ?		
	ources				Modules			▲ Severity		
	UnitsTable.cc				test40			Error	125 items	
			Messenger.cc; G4	InitsTab					120 Items	
		ectorAndUnit.cc	in lobben genee, e.		test40			Problem Data race	125 items	
	ctor.tcc				test40				125 Items	
	UlcontrolMes	senaer.cc			test40			Source	- 11	
	UlcontrolMes				test40			[Unknown]	3 items	
	UlcontrolMes	2			test40			DetectorConstruction.cc	20 items	
	UlcontrolMes				test40			enginelDulong.cc	2 items	
	UlcontrolMes				test40			G4AllocatorPool.cc	1 item	
	UlcontrolMes				test40			G4BlockingList.cc	1 item	
	UlcontrolMes				test40			G4DataVector.cc	2 items	
	UlcontrolMes				test40			G4DecayTableMessenger.cc	10 items	
	nknown]	Jengenee			test40			G4Element.cc	8 items	
-	st40.cc				test40			G4EventManager.cc	5 items	
Par					G4EvManMessenger.cc	17 items				
	st40.cc				test40			⊻ more		
					2			Module		
Data ra	ace: Observ	ations in Proble	m Set			Obs	ervations / Timeline	test40	125 items	
ID	Descrip 🔺	Source	Function	Module	State			State		
▶X1073			my_slave_thread		Not fixed			Not fixed	125 items	
▶X1097		test40.cc:58	G4_main		Not fixed					
▶X1101▶X1103		Itest40.cc:60 Itest40.cc:62	G4_main G4_main		Not fixed Not fixed					
▼X1239			my slave thread							
51										
	52 pid t myselfPid = gettid();									
	53 printf("The worker thread pid: %d\n", myselfPid);									
	54 threadRank = *(int *)rank_ptr;									
55										



Food for thought– loose propositions for possible future activities

> Expand scope of automated performance collection

- Every CPU has a performance monitoring unit that for the better part is unused
- Adopting a wide, common strategy for performance feedback
- Nightly build runs for instant performance feedback and regression monitoring
- Annotated source a la CMS (Peter Elmer)
- Background monitoring of batch servers for live and historical data
- Extending the availability of readily available performance monitoring C++ classes (Daniele Kruse)
- > Increasing the common availability of low level performance monitoring
 - Simplification of performance monitoring processes and outputs a long and hard task
- Most of the discussed scenarios could be deployed via our management system (possibly with Intel's help – if needed)
 - Some ideas already are on the table at openlab



Questions? Andrzej.Nowak@cern.ch