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Herbert Cornelius from Intel will give a computing seminar at CERN on Monday 6 February on high-throughput x86 computing (TFLOPS on a chip) [1]

Thursday, 26 January, 2012

In the context of the CERN openlab collaboration, Herbert Cornelius (Intel) will give an IT computing seminar at CERN on Monday 6 February, in the Council chamber at 16:00.

His talk will focus on many-cores technologies with a strong focus on the move to energy-efficient, high-throughput x86 computing (TFLOPS on a chip).

For more information, see http://cern.ch/Computing.Seminars [2]

Mélissa Gaillard, CERN openlab

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Description:

With Moore's Law alive and well, more and more parallelism is introduced into all computing platforms at all levels of integration and programming to achieve higher performance and energy efficiency. Especially in the area of High-Performance Computing (HPC) users can entertain a combination of different hardware and software parallel architectures and programming environments. Those technologies range from vectorization and SIMD computation over shared memory multi-threading (e.g. OpenMP) to distributed memory message passing (e.g. MPI) on cluster systems. We will discuss HPC industry trends and Intel's approach to it from processor/system architectures and research activities to hardware and software tools technologies. This includes the recently announced new Intel(r) Many Integrated Core (MIC) architecture for highly-parallel workloads and general purpose, energy efficient TFLOPS performance, some of its architectural features and its programming environment. At the end we will have a brief look at Exa-Scale computing, its challenges and opportunities.

About the speaker:

Dr. Herbert Cornelius is WW HPC Solution Architect at Intel with focus on technical, high-performance computing (HPC) and many-core computing. Before he was Engineering Manager in Intel's Cluster Software & Technologies group in EMEA, working on scalable parallel computing hardware & software solutions based on vectorization, multi-threading and message-passing utilizing multi-core/multi-processor cluster platforms. Before joining Intel, he served as Manager High-End Computing Europe at Fujitsu and worked at Cray Research from 1983 to 1990. He received a Ph.D. degree in Mathematics and Diploma degree in Mathematics and Informatics from Technical University of Berlin, Germany.

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