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For the next run of the LHCb experiment, new detectors are built, which use a different protocol from the one used for the old detectors in order to send the data collected from a collision. The data throughput will increase from the currently used 400 Gbit per second to astonishing 40 Tbit. The LHCb upgrade team built two FPGA boards: AMC40 and PCIe40 (see image 1.1). The AMC40 board has an Ethernet interface, produces UDP packets and sends them over the network. The PCIe40 board sends data over PCIe to a server, which in turn creates the network packets based on the PCIe data received, and sends them over the network. Each board is connected to the detectors and contains an FPGA, which does the preprocessing of the data received from the detector. The readout system is connected to the network and sends network packets to the backbone (see image 1.2). The readout system will operate at an overall speed of around 40 Tbit/s. In order to have a means of debugging all this network traffic, tools are necessary. The implementation of such a tool is the task for this Openlab Summer Student project.

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