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## New Vector/AVX2 Instructions in the Intel64 Instruction Set Architecture <sup>[1]</sup>

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[openlab III Minor Review](#) <sup>[2]</sup>

**Presentation file:**

 [New Vector\\_AVX2 Instructions in the Intel64 Instruction Set Architecture\\_SJarp.pdf](#) <sup>[3]</sup>

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[2] <https://indico.cern.ch/conferenceDisplay.py?confId=145165>

[3] [http://test-static-05.web.cern.ch/sites/test-static-05.web.cern.ch/files/presentations/New%20Vector\\_AVX2%20Instructions%20in%20the%20Intel64%20Instruction%20Set%20Architecture](http://test-static-05.web.cern.ch/sites/test-static-05.web.cern.ch/files/presentations/New%20Vector_AVX2%20Instructions%20in%20the%20Intel64%20Instruction%20Set%20Architecture)