Dynamically Adaptive Header Generator and Front-End Source Emulator for a 100 Gbps FPGA based DAQ

Marie Curie Fellow: Intel-CERN Doctorate Industrial Proaram

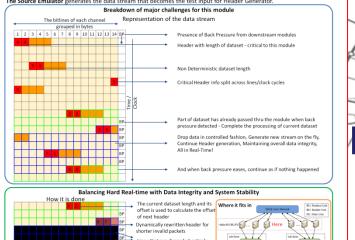
The Grand Challenge for proposed upgrade of LHCb experiment:

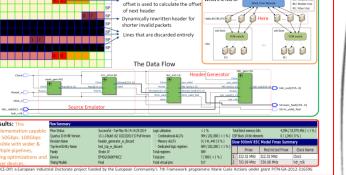
- 500 Data sources each generating data at 100 Gbps.
- Requires an FPGA DAQ module that

MAYNOOTH • handles data generated by the experiment. • dynamically adapt to potential inadequacies of other components.

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maintain real time operation while at the same time maintaining system stability and overall data integrity The Header Generator module is used to packetize the streaming data from the detector's Front-End electronics before it is sent to the PCs for further processing. The objective is to create a meta header or an index by creating packets out of 100s of small event dataset. This Header contains the total length of the packet, i.e. the sum of lengths of the individual datasets, the length of the largest dataset and a few other details calculated from information in the stream. The Source Emulator generates the data stream that becomes the test input for Header Generator





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RT 2014

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ICE-DIP is a European Industrial Doctorate project funded by the European Community's 7th Frameworkprogramme Marie Curie Actions under grant PITN-GA-2012-316596

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The Grand Challenge for proposed upgrade of LHCb experiment

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- Requires an FPGA DAQ module that
 - handles data generated by the experiment
 - dynamically adapt to potential inadequacies of other components
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What the poster talks about

Challenges specific to modules

- Those that are due to the data
- And those that arises due to the system

> The solution to these challenges

- Balancing the different needs (Real-Time, Data Integrity and Stability)
- The trade-offs accepted in achieving this balance

Discuss the results





2

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And the results

 Was 100 Gbps achieved? Resource usage? Visit Poster PS 3-27 to find out!



First Name and Family Name – ICE-DIP Project