This is an archive website with information on CERN openlab's fourth and fifth three-year phases (2012-2017)

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Unlock performance secrets of next-gen Intel hardware [1]

Date:
Tuesday, 12 May, 2015 - 15:30 to 16:30
Location:
CERN Building 31 IT Auditorium [2]
Software must be optimized for both threaded and SIMD vector parallelism to achieve scaled performance on modern machines. The gap (often 2 orders of magnitude) between modernized workloads and unoptimized baselines is increasing with every next hardware generation.
SIMD code modernization is not without cost, but exciting new features of OpenMP 4.0 "explicit vectorization" and new Intel® "Vectorization Advisor" software tool make it possible to introduce efficient and portable SIMD parallelism without disrupting ongoing development.
In addition to vector parallelism topic, the seminar will cover adjacent "code modernization" areas like new types of memory available in Next Generation Intel® Xeon Phi Product.
Indico or other event webpage:
For more information [3]

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Links
[1] http://test-static-05.web.cern.ch/news/unlock-performance-secrets-next-gen-intel-hardware
[2] https://maps.cern.ch/mapsearch/
[3] http://cseminar.web.cern.ch/cseminar/