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Benoit Dupont de Dinechin (KALRAY): High Performance Embedded Computing on the MPPA Single Chip Manycore [1]

Date:
Tuesday, 1 October, 2013 - 11:00 to 12:00
Location:
CERN, Building 513-1-024 [2]

The Kalray MPPA-256 processor integrates 256 processing engine (PE) cores and 32 resource management (RM) cores on a single 28nm CMOS chip. These VLIW cores are distributed across 16 compute clusters and 4 I/O subsystems, each with a locally shared memory. On-chip communications and synchronizations are supported by an explicitly addressed dual network-on-chip (NoC), with one node per compute cluster and 4 nodes per I/O subsystem. Besides external DDR, PCI and Ethernet, off-chip interfaces include a direct access to the NoC for low-latency processing of data streams.

The requirements of advanced embedded processing can be summarized as: high-performance; power efficiency; real-time processing; scalability; safety and reliability. In this presentation, we describe how the the Kalray MPPA MANYCORE architecture, and in particular the MPPA-256 processor, has been designed to meet those requirements. First, the MPPA MANYCORE is based on a single ISA (Instruction Set Architecture), like the Intel MIC or the Tilera, and unlike the TI Keystone or the NVIDIA Tegra. Second, the MPPA MANYCORE architecture includes a dual NoC that can be extended across processors in order to increase the number of compute clusters and I/O subsystems dedicated to an application. Third, the building blocks of the MPPA MANYCORE architecture are designed to support low-latency processing and accurate static timing analysis.

About the speaker

Benoit Dupont de Dinechin is the Chief Technology Officer at KALRAY [3], where he directs the software development group and is the architect of the KALRAY VLIW core. He brings more than 20 years of experience and technical expertise in software engineering, parallel computing, processor design and compiler tools development. National fellow at

STMicroelectronics, Benoit led the development of the ST120 VLIW-DSP core and the development of the production compiler of the VLIW family. Prior to join STM, Benoit served at Cray Research where he contributed to the Cray-T3E production compilers. Previously, he worked for the CEA where he was specialized in high performance computing. Benoit holds a PhD in Computer Science from the "Université de Paris 6", France, and a master?s degree from ENSAE, France. He was invited scientist at the McGill University, School of Computer Science, Canada. He authored more than 30 publications in conferences or technical journals and holds two patents.

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